Real-Time System Identification and Self-Tuning Control of DC-DC Power Converter Using Kalman Filter approach

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Abstract

Switch-mode power converters (SMPCs) are employed in many industrial and consumer devices. Due to the continuous reduction in cost of microprocessors, and improvements in the processing power, digital control solutions for SMPCs have become a viable alternative to traditional analogue controllers. However, in order to achieve high-performance control of modern DC-DC converters, using direct digital design techniques, an accurate discrete model of the converter is necessary. This model can be acquired by means of prior knowledge about the system parameters or using system identification methods. For the best performance of the designed controller, the system identification methods are preferred to handle the model uncertainties such as component variations and load changes. This process is called indirect adaptive control, where the model is estimated from input and output data using a recursive algorithm and the controller parameters are tuned and adjusted accordingly.

In the parameter estimation step, Recursive Least Squares (RLS) method and its modifications exhibit very good identification metrics (fast convergence rate, accurate estimate, and small prediction error) during steady-state operation. However, in real-time implementation, the accuracy of the estimated model using the RLS algorithm is affected by measurement noise. Moreover, there is a need to continuously inject an excitation signal to avoid estimator wind-up. In addition, the computational complexity of RLS algorithm is high which demands significant hardware resources and hence increase the overall cost of the digital system. For these reasons, this thesis presents a robust parametric identification method, which has the ability to provide accurate estimation and computationally efficient self-tuning controller suitable for real-time implementation in SMPCs systems.

This thesis presents two complete real-time solutions for parametric system identification and explicit self-tuning control for SMPCs. The first is a new parametric estimation method, based on a state of the art Kalman Filter (KF) algorithm to estimate the discrete model of a synchronous DC-DC buck converter. The proposed method can accurately identify the discrete coefficients of the DC-DC converter. This estimator possesses the advantage of providing an independent strategy for adaptation of each individual parameter; thus offering a robust and reliable solution for real-time parameter estimation. To improve the tracking performance of the proposed KF, an adaptive tuning technique is proposed. Unlike many other published schemes, this approach offers the unique advantage of updating the parameter vector coefficients at different rates. This thesis also validates the performance of the

identification algorithm with time-varying parameters; such as an abrupt load change. Furthermore, the proposed method demonstrates robust estimation with and without an excitation signal, which makes it very well suited for real-time power electronic control applications. Additionally, the estimator convergence time is significantly shorter compared to many other schemes, such as the classical Exponentially weighted Recursive Least Square (ERLS) method.

To design a computationally efficient self-tuning controller for DC-DC SMPCs, the second part of the thesis develops a complete package for real-time explicit self-tuning control. The novel partial update KF (PUKF) is introduced for real-time parameter estimation. In this approach, a significant complexity reduction is attained as the number of arithmetic operations are reduced, more specifically the computation of adaptation gains and covariance updates. The explicit self-tuning control scheme is constructed via integrating the developed PUKF with low complexity control algorithm such as Bányász/Keviczky PID controller. Experimental and simulation results clearly show an enhancement in the overall dynamic performance of the closed loop control system compared to the conventional PID controller designed based on a pre-calculated average model. Importantly, in this thesis, unlike a significant proportion of existing literature, the entire system identification, and closed loop control process is seamlessly implemented in real-time hardware, without any remote intermediate post processing analysis.

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Dedication

Dedicated to my mother, my brother Jomaa, my wife Khawla, and to the memory of my father.

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First and foremost, I am thankful to Almighty Allah for providing me with this opportunity and granting me the capability to proceed successfully.

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I also dedicate this PhD thesis to my two lovely daughters, Rateel and Fatma who are the pride and joy of my life. I love you more than anything and I appreciate all your patience and support during daddy's PhD studies. Finally, and most importantly, I do not know how, to begin with saying thank you to my soulmate, my dear wife Khawla. Your support, encouragement, quiet patience and unwavering love were undeniably the bedrock upon which the past four years of my life have been built. I understand it was difficult for you, therefore, I can just say thanks for everything and may Allah give you all the best in return.

Table of Contents

Abstract ..... **i**
Dedication ..... **iii**
Acknowledgment ..... **v**
Table of Contents ..... **vii**
List of Figures ..... **x**
List of Tables ..... **xiii**
List of Abbreviations ..... **xiv**
List of Symbols ..... **xvi**
Chapter 1 Introduction **1**
1.1 Introduction 1
1.2 Scope and Contribution of the Thesis- 3
1.3 Publications Arising from this Research 6
1.4 Layout of the Thesis 6
Chapter 2 Modelling and Control of DC-DC Switch-Mode Power Converters **8**
2.1 Introduction 8
2.2 Buck Converter Circuit 8
2.3 Steady-State Operation and Modelling of the Buck Converter 10
2.4 State-Space Average Model of Buck Converter in CCM 13
2.5 Open Loop Simulation Results 15
2.6 Closed-Loop Control for the PWM DC-DC Converter 17
2.7 Digital Control Implementation for PWM SMPCs 18
2.7.1 Digital Realisation of the Voltage-Mode Controlled Buck Converter 19
2.7.2 Digital Control Design Methods 21
2.7.3 Digital PID Controller 23
2.8 Direct Digital Control Design for Buck SMPC using Pole Placement 25
2.8.1 Overview 25
2.8.2 Simulation Results 27
2.9 Chapter Summary 33
Chapter 3 System Identification for DC-DC Converter **34**
3.1 Introduction 34
3.2 System Identification Procedure 34

3.3 Implementation Methods of System Identification 36
3.4 System Identification Techniques 36
3.4.1 Non-parametric System Identification 37
3.4.2 Parametric System Identification 39
3.5 Linear Model Structures for PEM 41
3.6 Parameter Estimation and Self-Tuning Control 44
3.7 Literature Review on System Identification for SMPC 45
3.7.1 Non-Parametric System Identification Methods for DC-DC Converters 46
3.7.2 Parametric Estimation Techniques for SMPC 50
3.8 Chapter Summary 54
Chapter 4 Parameter Estimation of DC-DC Power Converter Using Kalman Filter Approach 55
4.1 Introduction 55
4.2 Recursive Least Squares with Exponential Forgetting (ERLS) 56
4.3 The Disadvantages of ERLS Algorithm 59
4.4 Kalman Filter Algorithm Configured for Parameter Estimation 60
4.5 Kalman Filter Tuning in the Parametric Identification of SMPC 64
4.6 The Proposed Parametric Identification Scheme Using KF Approach 65
4.6.1 Pseudo-Random Binary Sequence (PRBS) 66
4.6.2 Model Structure Selection 68
4.7 Simulation Results for Steady-State Operation 69
4.9 Estimator Robustness Against Abrupt Load Change and the Absence of Excitation Signal 77
4.10 Chapter Summary 82
Chapter 5 A Computationally Efficient Self-Tuning Controller for DC-DC Switch Mode Power Converters Based on Partial Update Kalman Filter 83
5.1 Introduction 83
5.2 Partial Update Adaptive Filter Theory 84
5.3 Partial Update Methods 85
5.4 M-Max Algorithm 86
5.5 M-Max PUKF 87
5.6 Digital Self-Tuning Bányász/Keviczky PID Controller 90
5.7 Simulation Results 92
5.8 Chapter Summary 101

Chapter 6 Experimental Validation **102**
6.1 Introduction 102
6.2 Digital Signal Processor 102
6.2.1 Analog to Digital Converter (ADC) Module 103
6.2.2 Enhanced Pulse Width Modulation (ePWM) Module 104
6.3 Code Development Tool 105
6.4 Experimental Set-up of a Synchronous Buck Converter for Real-time Parameter Estimation and STC 105
6.5 Real-Time Parameter Estimation of DC-DC Converters using a Self-tuned Kalman Filter/ Experimental Validation 108
6.5.1 Real-Time Results for KF and ERLS 112
6.5.2 Model Validation 116
6.5.3 Abrupt Load Change / Real-Time Results 117
6.6 Experimental validation of the STC Design using the Developed M-Max PUKF 121
6.6.1 Parameter Estimation Using PUKF/ Real-Time Results 121
6.6.2 Improved Transient Response with Proposed STC 123
6.7 Chapter Summary 126
Chapter 7 Conclusion and Future Work **127**
7.1 Conclusion 127
7.2 Future Work 130
Appendix A Derivation of RLS Algorithm Based on Matrix Inversion Lemma **132**
Appendix B Simulink Model of the Proposed Structures **134**
Appendix C Developed Simulink Model for Real-Time Implementation **135**
References **136**

List of Figures

Figure 1.1 Explicit self-tuning control scheme in DC-DC converters 3
Figure 2.1 Circuit diagram of buck converter: a. non-synchronous buck converter, b. synchronous buck converter 10
Figure 2.2 Equivalent buck converter circuit during *On* state 11
Figure 2.3 Equivalent buck converter circuit during *Off* state 12
Figure 2.4 Open loop response of the SSA mode a. output voltage; b. inductor current 16
Figure 2.5 Frequency responses of the transfer function derived for the SSA model of the buck converter 16
Figure 2.6 Voltage mode control 17
Figure 2.7 Current mode control 18
Figure 2.8 Digital voltage-mode control of a synchronous Buck converter 20
Figure 2.9 PID controller in parallel form 24
Figure 2.10 PID controller in direct form 25
Figure 2.11 Closed loop control of the buck SMPC 26
Figure 2.12 Frequency response of the compensated and uncompensated DC-DC buck converter 29
Figure 2.13 Load transient response of the pole-placement controller during 50% step load change between 5 Ω and 2.5 Ω every 10 ms: a. output voltage; b. inductor current; c. load current 30
Figure 2.14 Pole-placement response during 80% load change between 5 Ω and 1 Ω every 10 ms, a: output voltage, b: inductor current, c: load current 32
Figure 3.1 Flowchart of system identification 35
Figure 3.2. Prediction error identification method 40
Figure 3.3 General-Linear Polynomial Model 41
Figure 3.4 ARX model structure 42
Figure 3.5 ARMAX model structure 43
Figure 3.6 BJ model structure 43
Figure 3.7 OE model structure 44
Figure 3.8 Explicit self-tuning control 44
Figure 4.1 An Adaptive Filter configured for system identification 56
Figure 4.2 Block diagram of the RLS approach 57

Figure 4.3 Kalman filtering structure 61
Figure 4.4 The Proposed parametric identification scheme using KF approach.....66
Figure 4.5 Nine-bits shift register with XOR feedback for 511 maximum length PRBS generation 67
Figure 4.6 The procedure of system identification.....71
Figure 4.7 Identification sequence: a. output voltage during ID; b. control signal during ID; c. ID enable signal.....72
Figure 4.8 On-line parameter estimation results using ERLS and KF: a. denominator coefficients; b. numerator coefficients; c. prediction error 74
Figure 4.9 Parameters estimation error; a. classical ERLS; b. KF 75
Figure 4.10 Adaptation gain for a_1 and b_1: a. ERLS; b. KF 76
Figure 4.11 On-line parameters estimation during a step load change from 5 Ω to 1 Ω at 0.02 s: a. output voltage; b. ERLS estimation; c. KF estimation.....78
Figure 4.12, Adaptation gain behaviour during abrupt load change: a. ERLS; b. KF 80
Figure 4.13, Estimator wind-up effect: a. PRBS injected for 5 ms; b.ID enabled for 80 ms; c. voltage model parameters ID.....81
Figure 5.1 System identification structure.....87
Figure 5.2 The proposed PU scheme.....89
Figure 5.3 Simplified closed-loop system for optimal design.....92
Figure 5.4 Explicit STC using M-Max PUKF.....93
Figure 5.5 Identification sequence: a. output voltage during enable 1 period; b. enable 2 signal for full KF; c. estimated model parameters using full KF.....94
Figure 5.6 On-line parameter estimation results using M-Max PUKF: a. denominator coefficients; b. Prediction error; c. Parameters estimation error 95
Figure 5.7 Transient response of the proposed STC with *de* =2 and K_D= 0.5: a. output voltage; b. inductor current; c. load current change between 0.66 A and 1.32 A every 10 ms.....97
Figure 5.8 On-line parameters estimation during a step load change from 5 Ω to 1 Ω at 0.05 s: a. Output voltage; b. PUKF estimation; c. Prediction error 99
Figure 6.1 Block diagram of TMS320F28335 103
Figure 6.2 Hardware overview of the experimental setup.....106
Figure 6.3 Block diagram of digitally voltage-controlled synchronous DC-DC buck converter 107

Figure 6.4 Generated PWM waveforms in the open loop test: a. output voltage with duty ratio 33%; b. the primary and secondary gate signals with 1μs dead time in a symmetrical case..... 108
Figure 6.5 Experimental output voltage during identification process..... 109
Figure 6.6. Experimental filtered data sampled at 20 kHz: a. output voltage; b. duty cycle. 110
Figure 6.7 Off-line parameter estimation using experimental data: a. model parameters; b. prediction error..... 111
Figure 6.8 Experimental output voltage during identification process with PRBS signal disabled after 10 ms..... 111
Figure 6.9 Real-time parameter estimation results using ERLS: a. denominator coefficients; b. numerator coefficients; c. steady state prediction error..... 113
Figure 6.10 Real-time parameter estimation results using KF: a. denominator coefficients; b. numerator coefficients; c. steady state prediction error..... 115
Figure 6.11 Residuals, cross-correlation function..... 116
Figure 6.12 Output voltage recorded on the DSP during a step load change from 5 Ω to 1 Ω at 50.015 s..... 117
Figure 6.13. Real-time parameters estimation during a step load change from 5 Ω to 1 Ω at 50.015 s: a. KF estimation, b. ERLS estimation..... 118
Figure 6.14 Adaptation gain behaviour during abrupt load change: a. KF; b. ERLS..... 120
Figure 6.15 Real-time parameter estimation results: a. denominator coefficients using M-Max PUKF; b. numerator coefficients using periodic PU KF..... 122
Figure 6.16 Transient response of the pole-placement PID controller with abrupt load change between 5Ω and 1Ω: a. 2 ms/div: showing two transient changes; b. 400 μs/div: “zoom-in”on second transient..... 124
Figure 6.17 Transient response of the explicit STC with abrupt load change between 5 Ω and 1 Ω: a. 2 ms/div showing two transient changes; b. 400 μs/div “zoom-in” on second transient..... 125
Figure B.1 Simulink model of parametric system identification using KF and STC based using PUKF..... 134

List of Tables

Table 2.1 Power stage parameters 15
Table 4.1 Classical RLS algorithm based matrix inversion lemma 58
Table 4.2 ERLS algorithm for time varying parameters 59
Table 4.3 Kalman filter recursive algorithm for state estimation. 62
Table 4.4 Kalman filter recursive algorithm for parameter estimation 63
Table 4.5 Bit cell setup for different MLBS generation 68
Table 5.1 Relative computational complexity of the proposed M-Max PUKF 89
Table 5.2 Relative computational complexity in terms of comparison 90
Table 5.3 Discrete time control-to-output transfer function identification 100
Table 5.4 Computational complexity reduction in the proposed STC scheme 100
Table 6.1 Parameters for the experimental synchronous buck converter 106
Table 6.2 Steady state parameter estimation comparison between ERLS and KF 114

List of Abbreviations

AC	Alternating Current
ADC	Analogue -to-Digital Converter
ARM	Advanced RISC Machines
ARMAX	Auto Regressive Moving Average Exogenous
ARX	Auto Regressive Exogenous
BBO	Biogeography-Based Optimization
BJ	Box-Jenkins
CCM	Continuous Conduction Mode
CPU	Central Processing Unit
CSS	Code Composer Studio
DAC	Digital-to-Analogue Converter
DC	Direct Current
DCD	Dichotomous Coordinate Descent
DCM	Discontinuous Conduction Mode
DFT	Discrete Fourier Transform
DPWM	Digital Pulse Width Modulation
DSP	Digital Signal Processor
DSPACE	Digital Signal Processor for Applied and Control Engineering
ELS	Extended Least Squares
ERLS	Exponentially Weighted Recursive Least Squares
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
GPIO	General-Purpose Input Output
IDE	Integrated Development Environment
IIR	Infinite Impulse Response
IRS	Inverse Repeat Binary Sequence
KF	Kalman Filter
LHP	Left Hand Plane
LMS	Least Mean Squares
LS	Least Squares
MA	Moving Average

MIMO	Multiple Input Multiple Output
MLBS	Maximum-Length Binary Sequence
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
NI USB	National Instrument Universal Serial Bus
NLMS	Normalised Least Mean Square
OE	Output Error
PC	Personal Computer
PEM	Prediction Error Methods
PI	Proportional-Integral
PID	Proportional-Integral-Derivative
PRBS	Pseudo Random Binary Sequence
PSD	Power Spectrum Density
PU	Partial Update
PUKF	Partial Update Kalman Filter
PWM	Pulsed Width Modulation
RAM	Random Access Memory
RLS	Recursive Least Squares
SCI	Serial Communications Interface
SFRA	Software Frequency Response Analyser
SID	System Identification
SISO	Single Input, Single Output
SMPC	Switch Mode Power Converter
SPI	Serial Peripheral Interface
SSA	State Space Average Model
STC	Self-Tuning Control
SW	Switch
UPS	Uninterruptible Power Supplies
VFF	Variable Forgetting Factor
VHDL	Verilog Hardware Description Language
WHT	Walsh-Hadamard Transformation
XOR	Exclusive OR
ZOH	Zero-Order-Hold

List of Symbols

f_s	Switching frequency
f_c	Corner frequency
G_{DC}	the steady-state gain
R_C	the parasitic resistances of the capacitor
R_L	the parasitic resistances of the inductor
R_o	Load resistor
v_C	Capacitor voltage
V_{in}	Input voltage
ω_0	power stage natural frequency
ω_{esr}	frequency location of the system zero
K_D	Derivative gain
K_I	Integral gain
K_P	Proportional gain
T_{sw}	Switching time
v_o	Output voltage
$\hat{y}$	Estimated output
δ_{ij}	Kronecker delta function
C	Capacitor
de	time delay steps
ε	Prediction error
e	Loop error
i_C	Capacitor current
i_L	Inductor current
i_O	Load current
L	Inductor
Q	Quality Factor
T_s	Sampling time
V_{ref}	Reference voltage
ξ	Damping factor
$d(k)$	Control signal
r	Noise variance

v	Observation noise
w	Model disturbance
θ	Parameters vector
λ	Forgetting factor
φ	Regression vector
μ	Step size
ϑ	Regulation parameter

Chapter 1 Introduction

1.1 Introduction

Switch-mode power converters are widely used in a variety of applications, ranging from DC motor drives, computers, home domestic appliances, spacecraft power systems and portable electronic devices [1]. All of these applications require efficient and cost-effective dynamic and steady-state power regulation over a wide range of operating conditions. Fixed-gain PID controllers are often used to achieve the required dynamic performance in these systems. However, poor knowledge of the power converter parameters may cause sub-optimal controller design. Moreover, unpredictable behaviour such as a sudden load variation, ageing of components, noise, and changes in operating mode may degrade the controller performance and potentially lead to instability of the system[2-4]. For instance, in SMPCs used in computers and laptops, the CPU must remain within its specified tolerance even when the processor performs a current-load step from a low current "sleep mode" to a high current "active mode" in a single clock cycle. This requires an efficient controller to be designed in order to achieve fast transient response.

Due to the aforementioned factors, adaptive and auto-tuning controllers based on system identification are now gaining more attention. These strategies are primarily feasible due to developments in digital control that offer many advantages over traditional analogue techniques. These include, but are not limited to robustness to noise and parameter variations, real-time programmability, component reduction, and simple integration with advanced techniques such as adaptive controllers and health monitoring diagnostics systems [4, 5].

Adaptive controllers often rely on reference models of the plant (transfer function, state-space). These models need to be accurate and are determined by system identification techniques. The identified model in discrete-time form, which is related to the analogue transfer function, is then used to tune the system controller. In addition, identifying converter parameters is useful from a maintenance and reliability point of view; particularly in on-line fault detection. In general, there are two main classes of system identification: parametric and non-parametric approaches. In the parametric approach, a system model is assumed, and the identification amounts to an estimation of the model parameters. On the other hand, non-parametric

identification methods estimate the frequency or impulse response of the system using spectral analysis and correlation analysis [4, 6]. From the literature, it is clear that non-parametric system identification does not require any prior knowledge of the system model [7]. However, due to significant algorithm execution time, non-parametric identification methods are often not suitable for use in on-line applications, particularly those exhibit highly dynamic characteristics. For this reason, parametric methods are typically more appropriate in applications where parameter estimation is integrated with a real-time controller [8].

In DC-DC converter applications, the load is often the most variable part of the system, which consequently affects the dynamics of the converter system. Hence, the load is usually regarded as a part of the system and is incorporated in the modelling and control design process.

In power electronics applications, both low cost and high performance are desirable. Therefore, there is a requirement for low computational complexity algorithms, which can be rapidly executed and exhibit fast convergence in parameter estimation in cases of a sudden load change or fault within the circuit. As a result, the impact of load variation can be minimised, since the new load value is estimated and taken into consideration in the controller design [9, 10]. This approach is called adaptive control and it has the ability to work continuously in estimating the converter parameters and update the controller in real-time. This type of compensation strategy provides considerable benefits such as better voltage stability, improved transient response, and design simplification [2]. Figure 1.1 shows the scheme of a typical self-tuning adaptive controller which, consists of two loops, an ordinary linear feedback compensator and the process to be controlled in the inner loop, while the outer loop is composed of a parameter estimator and a control design strategy. A recursive estimation algorithm is employed to update the regulator parameters once a new sample is available. In addition, an excitation signal is injected to enhance the parameter estimation results [11]. In the plant parameter estimation box, a fast and cost effective on-line estimation algorithm is required which can rapidly respond to any variation in components, providing the controller with the new values cycle by cycle to apply suitable settings. An apparent advantage of this strategy over other adaptive control approaches is that the system parameters are monitored and any fault can be diagnosed quickly and alleviated at an early stage; which is vital from a maintenance point of view. However, system identification and adaptive controller methods often impose a high computational burden and require relatively powerful processors to be implemented. Therefore, finding an algorithm with a high degree of accuracy, low

computational complexity, and fast parameter estimation convergence time is a particularly challenging task, and is the fundamental principle upon which this research work is based. .

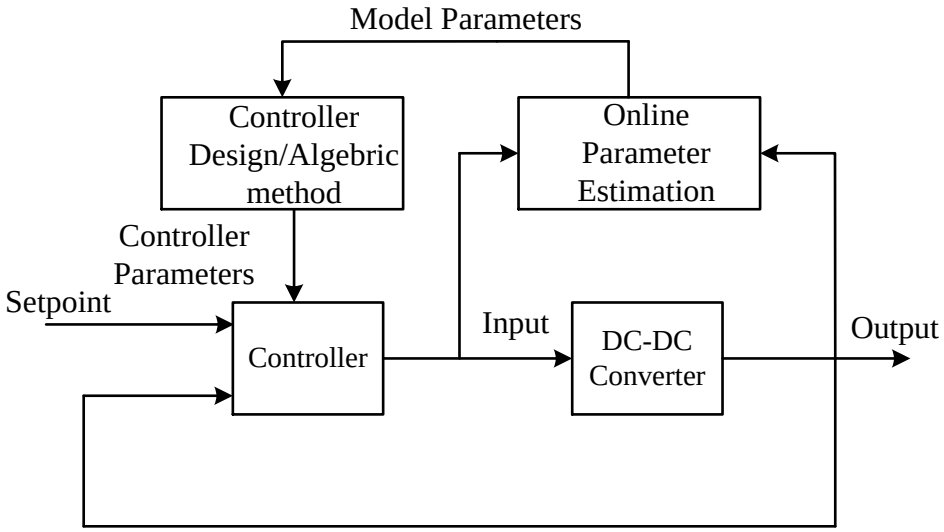


Figure 1.1 Explicit self-tuning control scheme in DC-DC converters

In recent years, system identification and adaptive control of DC-DC converters has received considerable interest amongst researchers in academia and industry. Generally, this field can be divided into the following broad categories:

1. System identification only; with no details about the computational cost of the method utilised and no real-time implementation.
2. Direct adaptive control; which does not involve parameter estimation in the tuning stage.
3. On-line estimation algorithms with trimmed computational cost; but which are not combined with an adaptive controller to evaluate system performance.

1.2 Scope and Contribution of the Thesis

This thesis is concerned with system identification and adaptive control of switch mode power supply applications. It specifically focuses on the synchronous DC-DC step-down converter. In such systems, low cost and high performance are key issues which must be considered.

According to the literature on existing on-line estimation algorithms, the recursive least squares (RLS) method is perhaps the most commonly used on-line parameter estimation

algorithm and is applied in many adaptive control designs. Unfortunately, the conventional RLS algorithm is only used to estimate fixed parameters, therefore, its implementation is rarely investigated experimentally in self-tuning control strategy for DC-DC power converters. To overcome this problem, the Exponentially weighted Recursive Least Square (ERLS) based upon a forgetting factor strategy is applied to estimate time-varying parameters in power converters, such as load change. However, in selecting the appropriate forgetting factor, there is always a trade-off between estimation accuracy and sensitivity to noise. Some modifications have been proposed to develop an adaptive forgetting factor, but the same trade-off is applicable [3].

In carrying out the research presented in this thesis, it is observed that the ERLS uses a scalar valued forgetting factor to give equal weight to all parameters in the system. This scenario is not ideal for the DC-DC converter where the transfer function parameters respond completely differently to any parameter change. Hence, this thesis presents a Kalman filter (KF) approach for parameter estimation of DC-DC power converters. It is believed that this is the first time a Kalman Filter has been used in this field. The KF strategy overcomes the previous described shortcomings of the classical ERLS and provides more degrees of freedom in optimising the identification process.

Importantly, and demonstrated via this thesis, the KF exhibits a different way to update the error covariance matrix, whereby a diagonal matrix is added. The diagonal elements of the matrix are chosen to reflect the size of the corresponding parameter variation in a random walk. Therefore, the error covariance matrix will no longer tend to zero. In this updated form, the gain vector is kept as a non-zero value. Thus, the parameter vector changes continually at different rates. Considering the process noise covariance matrix as a design variable adds more flexibility to the KF. This characteristic assumes that there are different variations in different parameters, which is exactly the case in system identification of DC-DC converters when the effect of load change is studied. Since the KF follows the same initialisation technique used for ERLS, the process noise covariance matrix and measurement noise variance remain as the problematic parameters which need to be set by the designer, and this limits the adaptive behaviour of the algorithm.

To overcome this problem, a new iterative algorithm based on the innovation term is proposed to produce a novel self-tuned KF. The diagonal matrix obtained is used to improve the tracking ability of the filter in the event of any abrupt load change. Additionally, unlike

classical RLS methods, the KF approach demonstrates robust estimation with and without any excitation signal due to the linear scheme used to update the gain covariance matrix. This makes the KF approach very well suited for real-time power electronic control applications.

In cost sensitive applications like a DC-DC converter, computational burden is a critical factor. Thus, a novel partial update Kalman filter (PUKF) is presented in this research to reduce the computational complexity of the classical KF. The concept of this algorithm is based on data vector analysis to select the most important subset of the adaptive filter coefficients to be updated on a cycle-by-cycle basis. The robustness of the estimation results is investigated through designing an on-line adaptive controller. A stable and well-regulated output voltage is achieved. Importantly, the computational burden on the microprocessor platform is reduced by 50% compared to the full update KF. With minimum number of arithmetic operations, the self-tuning digital Bányász/Keviczky PID controller is chosen as the main voltage controller in a proposed Self Tuning Controller (STC) scheme. The dynamic performance of the controller and the developed estimator are investigated in detail. The on-line results validate the feasibility of the proposed PUKF approach in parameter estimation for DC-DC converters as the parameter variation are detected and estimated quickly and accurately. The proposed controller has the ability to work continuously in the feedback loop and rapidly regulates the output voltage after abrupt load changes.

In summary, the main objectives and contributions to knowledge of this research are as follows:

1. To Investigate the Kalman filter for parameter estimation in DC-DC converters (believed to be for the first time in this field).
2. To develop a novel self-tuned Kalman filter for time-varying parameter estimation.
3. To propose a novel partial-update Kalman filter as an efficient replacement for the existing ERLS with lighter computational cost.
4. To develop a computationally efficient self-tuning control scheme suitable for low cost, low power DC-DC converters.
5. To implement and validate the proposed algorithm in simulation, and experimentally using a Texas Instruments TMS320F28335 DSP platform, Embedded Coder Support, and a synchronous DC-DC buck converter.

1.3 Publications Arising from this Research

1. **M. Ahmeid,** M. Armstrong, S. Gadoue, M. Algreer, and P. Missailidis, "Real- Time Parameter Estimation of DC-DC Converters using a Self-tuned Kalman Filter," IEEE Transactions on Power Electronics, vol. PP, pp. 1-1, 2016.
2. **M. Ahmeid**, M. Armstrong, S. Gadoue, and P. Missailidis, "Parameter estimation of a DC-DC converter using a Kalman Filter approach," in Power Electronics, Machines and Drives (PEMD 2014), 7th IET International Conference on, 2014, pp.
3. **M. Ahmeid**, M. Armstrong, S. Gadoue, M. Algreer, and P. Missailidis "Computationally Efficient Self-Tuning Controller for DC-DC Switch Mode Power Converters Based on Partial Update Kalman Filter", under review in the IEEE Transactions on Power Electronics.

1.4 Layout of the Thesis

This thesis is organised as follows:

Chapter 2 presents DC-DC power converter topologies, modelling, and control. In particular, operation and circuit configuration of buck DC-DC SMPCs. The derivation of the state-space average model is also introduced, followed by simulation results of an open-loop buck converter operating in Continuous Conduction Mode (CCM). It also provides an overview of control strategies applied to regulate the output voltage with more emphasis on digital voltage mode control structure. In the digital control section, design by emulation and direct digital design methods are outlined and discussed in detail. Among these methods, the pole-placement approach is adopted and a digital PID controller is designed and tested in simulation. The modelling and control in this chapter is used to evaluate the proposed algorithms for system identification and self-tuning control.

Chapter 3 reviews the principles and methods of system identification. It also provides details on the main steps followed in the identification procedure. In parametric identification approaches, the commonly applied model structures are highlighted. In addition, the self-tuning adaptive control strategy is also demonstrated. Moreover, a literature survey on recently

published research on system identification /adaptive control techniques for DC-DC SMPCs are also reviewed in this chapter.

Chapter 4 provides details on the adaptive algorithms used in the area of parametric system identification with more focus on the derivation of the classical LS and RLS algorithms. This is followed by introducing the proposed KF approach configured for on-line system identification. Analysis and derivation of the proposed algorithm is also demonstrated. Furthermore, Chapter 4 explores a new tuning method for KF based on innovation term to detect and estimate the fast changes in the system. The new identification schemes in this chapter are comprehensively tested and validated through simulations.

Chapter 5 presents the proposed PUKF. The first part of this chapter provides details on partial update adaptive filters and the methods applied in this scheme. Following this, an overview of M-Max PU method is presented along with the derivation of the M-Max PUKF adaptive algorithm. In addition, Chapter 5 demonstrates the effectiveness of using the proposed PUKF in a complete package of explicit STC. Extensive simulation results that evaluate the performance of the PUKF and the proposed self-tuning control scheme are provided in this chapter.

Chapter 6 focuses on the experimental validation of the developed adaptive algorithms for system identification and self-tuning control using a high speed microprocessor board. It presents an overview on the architecture of the selected digital signal processor platform. Importantly, Chapter 6 concentrates on the real-time implementation of the proposed KF and PUKF employed in STC scheme. It also provides a comparison between the obtained experimental results of the proposed scheme using the full update KF and the classical ERLS algorithm. In addition, the proposed PUKF is investigated in real-time STC structure and the overall performance is compared with the conventional digital PID controller.

Finally, Chapter 7 presents the conclusion drawn for this thesis and it summarises possible suggestions for future work.

Chapter 2 Modelling and Control of DC-DC Switch-Mode Power Converters

2.1 Introduction

Switch-mode power converters are widely used in a variety of applications, ranging from Megawatts variable speed motor drives, several hundred-watt power supplies for computers and office equipment, to milliwatt converters for portable battery operated devices. All of these applications require efficient and cost-effective dynamic and steady-state power regulation over a wide range of operating conditions [12, 13]. Generally, in DC-DC converters, electronic switches (transistors, diodes) and storage components (capacitators, inductors) are utilised to transfer energy from the DC voltage source to a load. This process produces DC output voltages smaller or greater in magnitude than the DC input voltage. The resultant output voltage depends on how the passive and active components are configured, and the method of control [13, 14]. Typically, the output voltage is regulated, and kept constant regardless of any variations in input source or load current. In practical applications, such as portable personal computers, several DC-DC converter topologies may be connected to a single DC power source (e.g. Lithium Ion battery). Buck, Boost, Buck-Boost, and Flyback are common conventional topologies.

In this thesis, the research work will focus on the Buck converter only. This converter is widely used in industry, and is regularly adopted in academic literature. [13]

2.2 Buck Converter Circuit

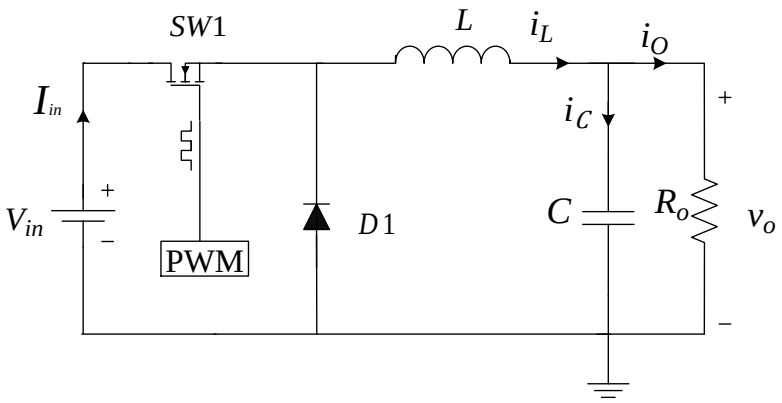
The buck converter, sometimes called the step-down converter, is one of the simplest and most commonly used power converter topologies. The traditional or non-synchronous buck converter circuit as presented in figure 2.1(a) consists of DC power supply, a power switch (*SW1*) (*e.g.* MOSFET) connected to the high side, a freewheeling diode *D1* connected to the ground, and an output filter constructed from an inductor *L* and capacitor *C*. Pulse Width Modulation (PWM) is applied to switch the MOSFET (*SW1*) on and off repeatedly every switching period T_{sw}. This will charge and discharge the storage components *L* and *C* and deliver the energy to the load resistor R_o [13]. To avoid high ripples in the regulated output

voltage, the corner frequency for the output filter f_c is recommended to be much lower than the converter switching frequency f_s. The corner frequency can be calculated based on the inductor and capacitor values as presented in (2.1).[15].

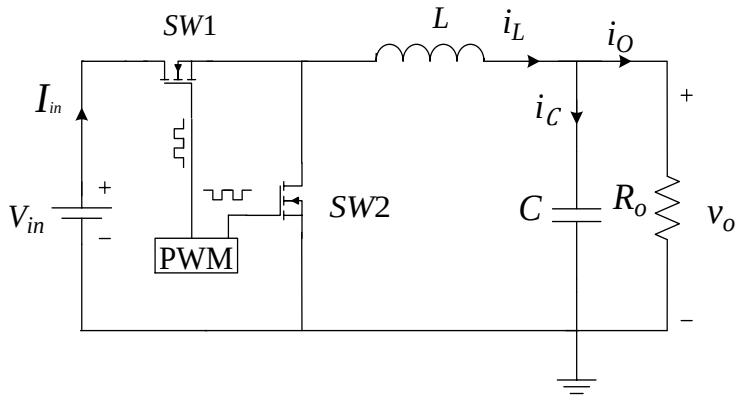
$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{2.1}$$

By assuming ideal components and converter steady-state operation, the relationship between the input voltage V_{in} and the output voltage v_{out} can be expressed as $v_{out} = V_{in} \times D$, where D is the controllable duty cycle of the semiconductor switch [15]. This converter configuration has two distinct operating modes. In the first mode, the current flows through the inductor continuously and never drops to zero over the entire switching period T_{sw}; this mode is called Continuous Conduction Mode (CCM). On the other hand, the second operational mode appears when the inductor current drops to zero for a proportion of the switching cycle, and as a result the diode *D1* will not conduct. This mode is called Discontinuous Conduction Mode (DCM) [12-14].

Since the buck power stage has gained significant attention in low voltage applications of less than 5V, the voltage drop across the freewheeling diode *D1* can no longer be ignored. Therefore, another variation of the buck power stage known as a synchronous-buck power stage is typically adopted; as shown in figure 2.1(b). In the synchronous buck converter, the freewheeling diode is replaced by a second active switch (*SW2*) [16]. Regardless of the cost, the synchronous converter enhances the overall efficiency of the system by lowering the power loss caused by the diode [17]. Therefore, this type of converter is a common choice in power supply design and is popular in the PC market [14].



(a)



(b)

Figure 2.1 Circuit diagram of buck converter: a. non-synchronous buck converter, b. synchronous buck converter

2.3 Steady-State Operation and Modelling of the Buck Converter

Developing a system model is a typical requirement in closed-loop feedback controllers. This allows the designer to evaluate the operation of the system in detail and, if necessary, understand the impact of sensitivity to variation in individual parameters or components. Furthermore, it facilitates greater investigation into the performance of systems such as power converters, which exhibit different operational modes in steady-state [18].

Figures 2.2 and 2.3 illustrate the two states of a buck converter operating in CCM. In this circuit diagram, the parasitic resistances of the inductor and capacitor (R_L, R_C) are included in the analysis to model the practical losses in the converter power stage. During the *On* state, the switch *SW1* is connected and switch *SW2* is turned off, causing a linear increase in the inductor current and energy being stored in the inductor. The time duration of the *On* state T_{on} is equal to $D \times T_{sw}$, where *D* denotes the duty ratio.

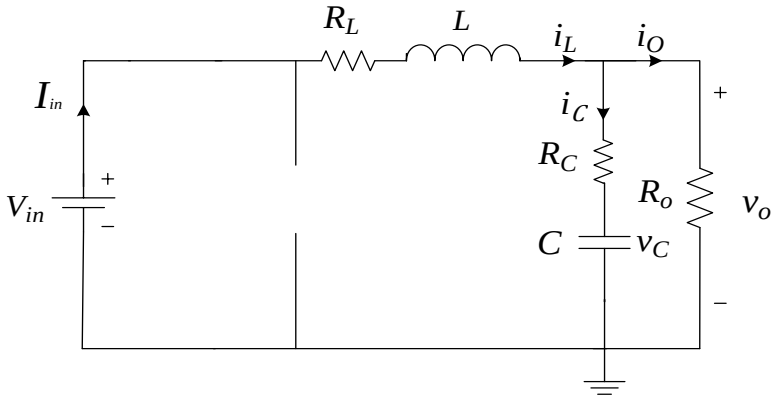


Figure 2.2 Equivalent buck converter circuit during *On* state

In order to describe the converter dynamics during the *ON* state, Kirchhoff's current and voltage laws are applied, and the following differential equations are obtained

$$\frac{di_L}{dt} = \frac{1}{L}(V_{in} - (R_L + R_C)i_L - v_C + R_C i_o) \tag{2.2}$$

$$\frac{dv_C}{dt} = \frac{1}{C}(i_L - i_O) = \frac{1}{C}(i_L - \frac{v_o}{R_o}) \tag{2.3}$$

$$v_o = R_C(i_L - i_o) + v_C = R_C C\frac{dv_C}{dt} + v_C \tag{2.4}$$

Equations (2.2) – (2.4) are usually rearranged in matrix form as a linear set of state-space equations describing the topological *On* state [19]:

$$\frac{dx}{dt} = A_1 x + B_1 V_{in} \tag{2.5}$$

$$\begin{bmatrix} \dot{v}_C \\ \dot{i}_L \end{bmatrix} = \begin{bmatrix} \frac{-1}{C(R_C+R_o)} & \frac{R_o}{C(R_C+R_o)} \\ \frac{-R_o}{L(R_C+R_o)} & \frac{-1}{L}\left(\frac{R_o R_C}{R_C+R_o} + R_L\right) \end{bmatrix} \begin{bmatrix} v_C \\ i_L \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix} V_{in} \tag{2.6}$$

The output voltage matrix is expressed as:

$$y = C_1 x + E_1 V_{in} \tag{2.7}$$

$$[v_o] = \begin{bmatrix} \frac{R_o}{(R_C+R_o)} & \frac{R_o R_C}{(R_C+R_o)} \end{bmatrix} \begin{bmatrix} v_C \\ i_L \end{bmatrix} + [0] V_{in} \tag{2.8}$$

In the state-space representation in (2.6) and (2.8) the state variable vector x includes the capacitor voltage v_C, and the inductor current i_L $[v_C \quad i_L]^T$, y represents the output voltage v_o,

and the matrices A_1,B_1,C_1, and E_1 define the vectors and matrices of the converter during this interval.

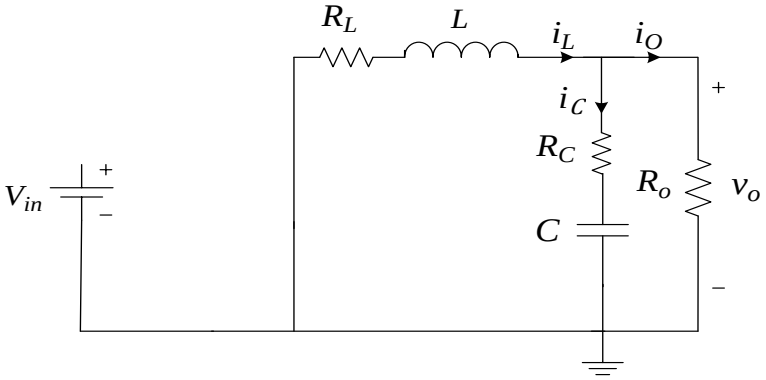


Figure 2.3 Equivalent buck converter circuit during *Off* state

After a short dead time, switch *SW1* is open and switch *SW2* is closed with time duration equal to $(1-D)\times T_{sw}$ (*Off* state) as shown in figure 2.3; at which point the voltage source is disconnected and the inductor current falls linearly. Similarly, the mode of operation during the *Off* state is described by state-space representation with system vectors and matrices identical to the *On* duration except for the control vector *B*, which is now equal to zero since the input voltage is disconnected. In both cases, the model is called a large signal model [18, 19]. After the switching period T_{sw} is completed, the switch *SW1* is on and *SW2* is off again [13]. Referring to figure 2.3 the state equations during the *Off* state are given by:

$$\frac{di_L}{dt} = \frac{1}{L}\left(- (R_L+R_C)i_L - v_C + R_C i_o\right) \tag{2.9}$$

$$\frac{dv_C}{dt} = \frac{1}{C}(i_L - i_O) = \frac{1}{C}\left(i_L - \frac{v_o}{R_o}\right) \tag{2.10}$$

$$v_o = R_C(i_L - i_o) + v_C = R_C C\frac{dv_C}{dt} + v_C \tag{2.11}$$

By arranging (2.9) and (2.10) in a matrix form the state space representation of the buck converter during the off state is introduced as follows:

$$\begin{bmatrix} \dot{v}_C \\ \dot{i}_L \end{bmatrix} = \begin{bmatrix} \dfrac{-1}{C(R_C+R_o)} & \dfrac{R_o}{C(R_C+R_o)} \\ \dfrac{-R_o}{L(R_C+R_o)} & \dfrac{-1}{L}\left(\dfrac{R_o R_C}{R_C+R_o}+R_L\right) \end{bmatrix} \begin{bmatrix} v_C \\ i_L \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_{in} \tag{2.12}$$

$$\frac{dx}{dt} = A_2 x + B_2 V_{in}$$

Similarly the output equation during *Off* duration can be written as:

$$[v_o]=\begin{bmatrix}\frac{R_o}{(R_C+R_o)} & \frac{R_oR_C}{(R_C+R_o)}\end{bmatrix}\begin{bmatrix}v_C\\ i_L\end{bmatrix}+[0]V_{in}$$

$$y=C_2x+E_2V_{in} \tag{2.13}$$

2.4 State-Space Average Model of Buck Converter in CCM

According to the two states presented in the previous section, the transient analysis and design of an appropriate controller for simple buck converter is not a trivial task, due to the complicated equations which need to be solved. In order to reduce this complexity and to find a linear model for the DC-DC converter, these two states can be combined and averaged using knowledge of the duty ratio, *D*. The result is the following averaged large signal state model or the State Space Average Model (SSA) equations [13, 19]:

$$\begin{aligned}\frac{dx}{dt}&=Ax+BU\\ y&=Cx+EU\end{aligned} \tag{2.14}$$

where

$$\begin{aligned}A&=dA_1+(1-d)A_2\\ B&=dB_1+(1-d)B_2\\ C&=dC_1+(1-d)C_2\\ E&=dE_1+(1-d)E_2.\end{aligned} \tag{2.15}$$

Due to the switching behaviour of the converter the large signal model indicated by plain lower case can be expressed in terms of the steady value in upper case and the small signal with tilde notation and given by:

$$\begin{aligned}x&=X+\tilde{x}\\ d&=D+\tilde{d}\\ y&=Y+\tilde{y}\\ u&=U+\tilde{u}\end{aligned} \tag{2.16}$$

By substituting (2.15-2.16) in (2.14), and discarding the higher order terms, the AC small-signal description is obtained and given by:

$$\begin{aligned}\dot{\tilde{x}} &= [DA_1+(1-D)A_2]\tilde{x}+[DB_1+(1-D)B_2]\tilde{u}+[(A_1-A_2)X+(B_1-B_2)U]\tilde{d}\\ \tilde{y} &= C\tilde{x}+E\tilde{u}+[(C_1-C_2)X+(E_1-E_2)]\tilde{d}\end{aligned} \tag{2.17}$$

Finally, by applying the Laplace transformation to the AC equation (2.17), the transfer function between the output voltage and the duty ratio is expressed as [19]:

$$G_{dv}(s)=\frac{v_o}{D}\left[\frac{(CR_Cs+1)}{s^2LC\left(\frac{R_C+R_o}{R_L+R_o}\right)+S\left(CR_C+C\left(\frac{R_OR_L}{R_O+R_L}\right)+\frac{L}{R_O+R_L}\right)+1}\right] \tag{2.18}$$

The derived control to output transfer function in (2.18) can be expressed in the standard form of a second order transfer function [20]:

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)}=G_{DC}\frac{1+\frac{s}{\omega_{esr}}}{1+\frac{s}{Q\omega_0}+\left(\frac{s}{\omega_0}\right)^2} \tag{2.19}$$

where ω_0 is the power stage natural frequency, Q is the quality factor, G_{DC} is the steady-state gain, and ω_{esr} is the frequency location of the system zero due to equivalent series resistance of the capacitor R_c . For the buck converter, these figures are computed by equating (2.18) and (2.19) as follows [2]:

$$\begin{aligned}\omega_0 &= \sqrt{\frac{R_o+R_L}{LC(R_o+R_C)}}\\ G_{DC} &= V_{in}=\frac{V_o}{D}\\ Q &= \frac{1}{\omega_0\left(R_CC+\frac{R_oR_LC}{R_o+R_L}+\frac{L}{R_o+R_L}\right)}\\ \omega_{esr} &= \frac{1}{CR_C}\end{aligned} \tag{2.20}$$

In equation (2.19), the quality factor Q is used to measure the dissipation in the system, which is introduced by another term, (ξ), which is called damping factor where $Q = 1/2\xi$. This factor indicates the amount of overshoot during the transient response. In addition to the quality factor Q, the two Left Hand Plane (LHP) poles introduced in (2.19) are directly related to the corner frequency ω_0, and hence the dynamic behaviour of the converter. Moreover, a LHP zero is observed which depends on the equivalent series resistance of the output capacitor R_C. This

zero may lead to increased overshoot and make the system faster. In DC-DC converters, excessive overshoot is normally undesirable; therefore, designing a controller that can cancel the effect of this zero is usually preferred.

2.5 Open Loop Simulation Results

After the modelling step is completed, simulating the derived mathematical model of the buck converter is recommended in order to investigate the behaviour of the system. To carry out this procedure, a simulation package such as MATLAB/SIMULINK is used. In this research, the verification is performed in a 10 V to 3.3 V synchronous buck converter switched at 20 kHz, with selected power stage parameters listed in Table 2.1. This prototype converter has been designed by Algreer [8] and adopted in this work without change.

Table 2.1 Power stage parameters

Symbol and description	Parameter
L: output inductor	220 μH
C: output capacitor	330 μF
R_C: equivalent series resistor	25 mΩ
R_L: inductor series resistance	63 mΩ
R_o: load resistance	5 Ω

The open loop waveforms of the inductor current and the output voltage obtained from the Simulink model of the buck converter is illustrated in figure 2.4. It is shown here that the switching ripples are periodically repeated every switching cycle. In addition, the frequency response of the transfer function, derived in (2.18), is commonly used to investigate the dynamic characteristics of the converter for control design purposes. Figure 2.5 depicts the frequency response of the open-loop converter. From this plot, the important terms which describe the stability and dynamic behaviour of the converter, such as damping factor, phase margin, and gain margin, can be extracted and as a result an appropriate controller may be designed to meet the desired specifications.

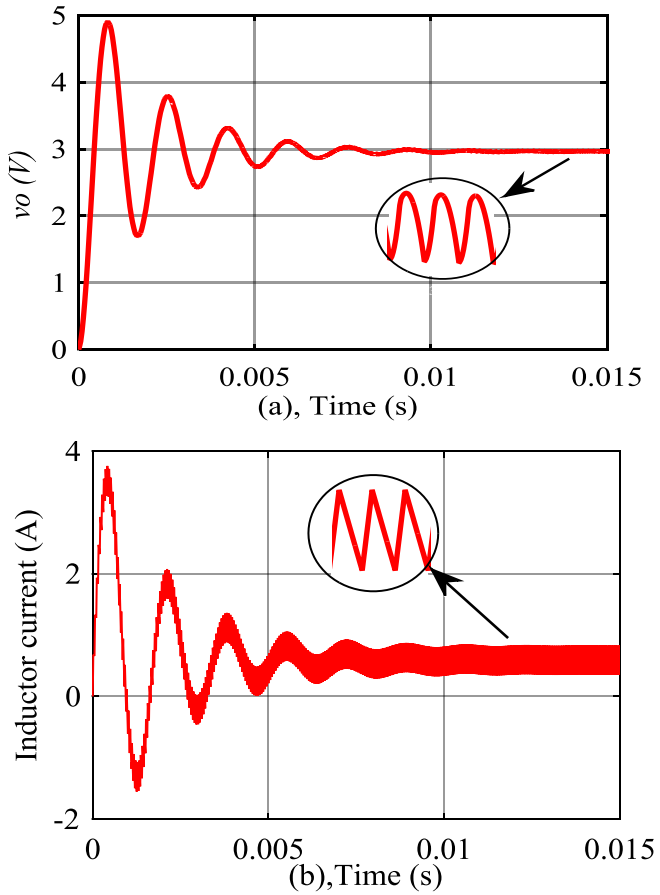


Figure 2.4 Open loop response of the SSA mode a. output voltage; b. inductor current

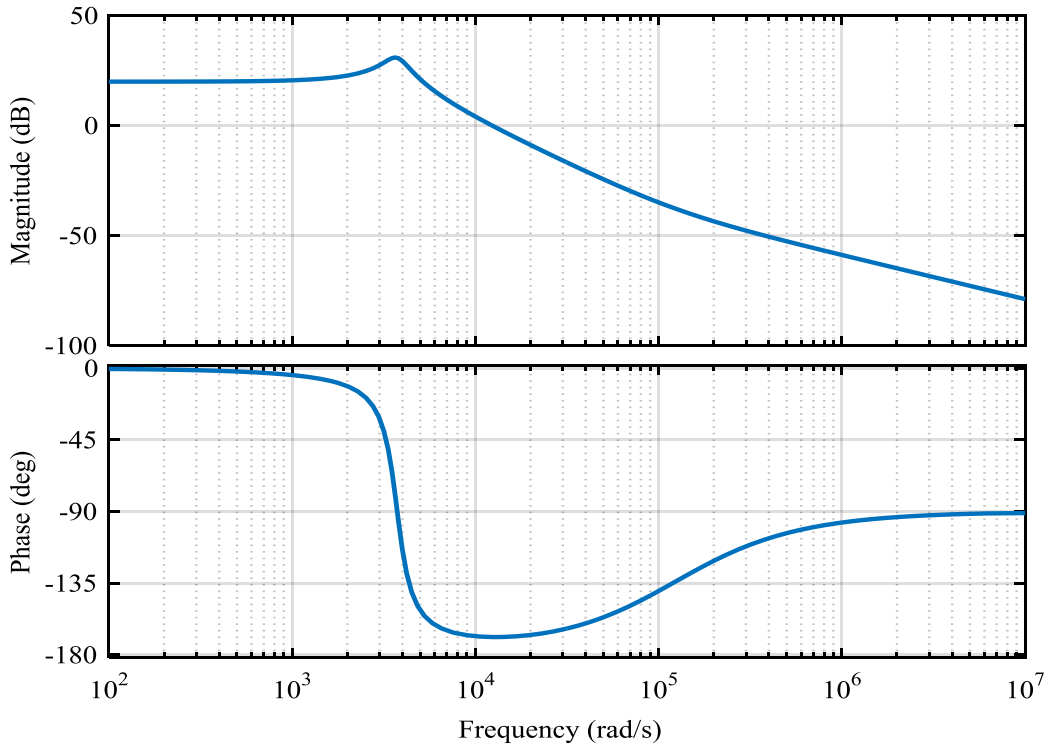


Figure 2.5 Frequency responses of the transfer function derived for the SSA model of the buck converter

2.6 Closed-Loop Control for the PWM DC-DC Converter

In the previous section, the duty cycle is set to a constant value (0.3). However, this situation is not practical since the converter often faces disturbances such as load current change, input voltage change, and tolerance in the circuit parameter values. Consequently, the output voltage will not stay at the desired value under all operating conditions. Therefore, the use of negative feedback control is essential to keep the output voltage at the reference value V_{ref} regardless of any disturbance which occurs while the converter is operating. Typically, output variation is allowed within a specified range when any step change in load current or reference voltage is applied [12].

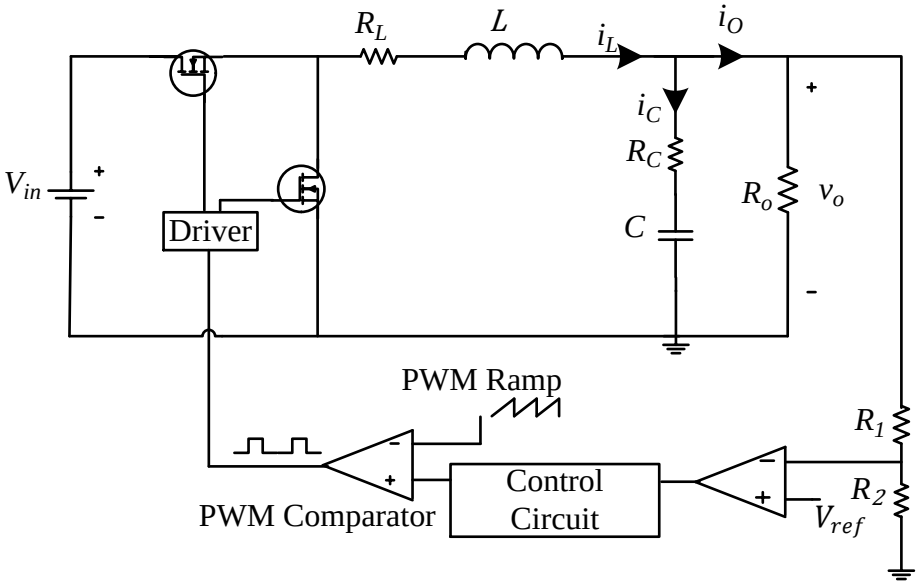


Figure 2.6 Voltage mode control

The negative feedback control is implemented in two types of compensation scheme: voltage mode control, and current mode control. In voltage mode control structure (figure 2.6), only a single loop is required to sense the actual output voltage and compare it with the reference voltage, and then the error signal is fed to the compensator for PWM duty cycle generation. Due to the single feedback path required in voltage mode control, a simple design and analysis of the converter controller is achieved. Moreover, the low cost in sensing the output voltage simply using a voltage divider is introduced in this mode which adds more advantages in practical implementation. However, some drawbacks have emerged in voltage mode control in

terms of slow responses to any change in the output voltage or line voltage, because the feedback voltage is measured on the output capacitor[21].

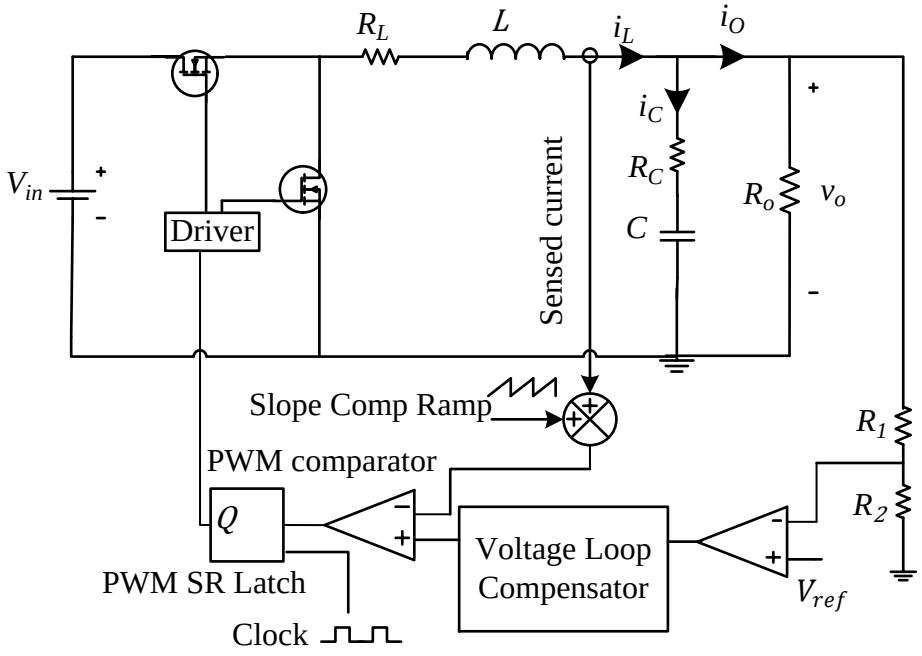


Figure 2.7 Current mode control[22]

In current mode control (figure 2.7), the indirect regulation of the output voltage is achieved by providing cycle-by-cycle control of the current. In this topology, the inductor current rises with a slope determined by V_{in} -v_o, this waveform will respond immediately to line voltage changes, eliminating both the delayed response and gain variation with changes in input voltage. In addition, in current mode control a higher bandwidth gain is obtained as the effect of the output inductor is minimised and the filter now offers only a single pole to the feedback loop. Consequently, the response to line and output voltage change become faster than in voltage mode control. However, in this mode, inner and outer loops are constructed, and hence the complexity and cost of the structure are increased [21].

2.7 Digital Control Implementation for PWM SMPCs

The control schemes described in the previous section are classically implemented using analogue controllers. Simply, the analogue controllers are constructed from a combination of passive components, such as capacitors, resistors, and op-amplifiers. These elements are prone

to change due to ageing and environmental variations, and they contribute to power dissipation and often occupy a large footprint on a printed circuit board. In addition, circuit redesign is required if any parameter or design specification is changed, which increases cost and consumes development time [23].

In the last 20 years, digital control has gradually found its way into power electronics applications because of the rapid decrease in cost, and enhanced performance, of digital signal processors. Digital controllers offer many advantages over their analogue counterparts, including the ability to implement more advanced control schemes such as sophisticated non-linear control algorithms, adaptive control systems, and parameter estimation/system identification algorithms. As a digital control system is mainly software-based, the number of passive components used are reduced, and therefore the system becomes less susceptible to noise and is smaller. Another advantage of digital controllers is that they can monitor and interact with the application while it is operating, which is not possible with analogue control. Most importantly, the design flexibility is introduced, where the same design platform is used for different topologies with the only modification being needed is in the application code [4, 24-26]. Although there are many strengths of digital control systems, however, some drawbacks can be observed, such as the computational time delay due to the control algorithm, lower control loop bandwidth compared with analogue control systems, and finite word length in the processor which can cause limited signal resolution and limit cycle oscillation [25, 27, 28].

2.7.1 *Digital Realisation of the Voltage-Mode Controlled Buck Converter*

The voltage mode control scheme is widely adopted to regulate the output voltage, due to its simplicity and cost effectiveness. To ensure high performance digital control for the SMPC, three basic hardware blocks are employed: the analogue-to-digital converter (ADC) block, the digital compensator, and the Digital Pulse Width Modulation (DPWM) block which works as the digital-to-analogue converter (DAC) [18, 29, 30]. These blocks are connected to the input and output of the converter through analogue components such as the gate drive and the sensor or voltage divider. Figure 2.9 illustrates the combination of analogue and digital parts used to establish voltage mode control.

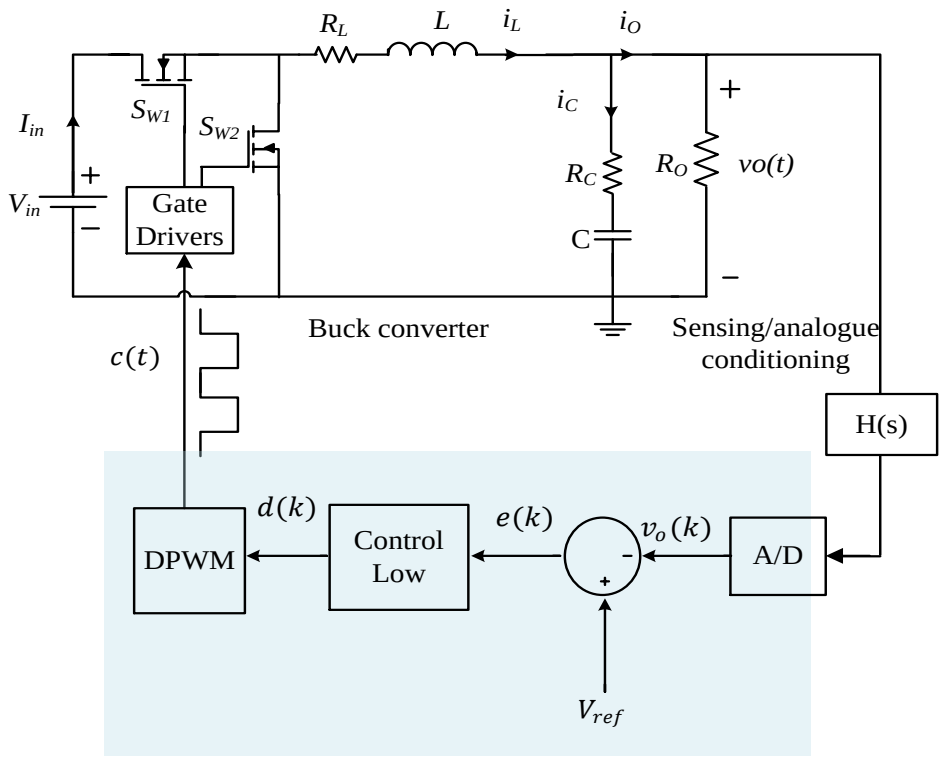


Figure 2.8 Digital voltage-mode control of a synchronous Buck converter

As depicted in figure 2.8 a voltage-divider circuit is used to sense and scale down the measured output voltage, and this provides the ADC with a suitable input voltage which matches its electrical characteristics within a specified range. Therefore, the ADC is protected by attenuating any measured voltage which exceeds its dynamic scale. For greater protection and isolation, a buffer circuit with wide bandwidth and an anti-aliasing filter (low pass filter) are often interposed between the voltage divider circuitry and the analogue input pins of the ADC module[29].

To guarantee accurate digital representation of the measured continuous voltage, the cut-off frequency of the anti-aliasing filter should be lower than half of the ADC sampling frequency according to the Nyquist-Shannon sampling theorem [31]. In order to maintain the desired voltage regulation, the selected ADC must have certain important features such as that the resolution of the ADC should be less than the maximum allowed voltage fluctuation. Thus, any sensed voltage higher than this limit is digitized and considered in the compensation scheme. Furthermore, the ADC speed is vital to accomplish rapid conversion and a well-regulated output voltage with improved dynamic response [32, 33].

After the sensed output voltage is digitized $v_o(k)$, the digital error signal $e(k)$ is computed through subtracting $v_o(k)$ from the constant digital value, V_{ref}, corresponding to the desired output voltage. Then, this error is minimised by the action of the central discrete controller by generating the appropriate control signal $d[k]$ [18, 24, 27, 34]. Linear and non-linear controllers can be employed in this role. In case of linear controllers, the well-known digital proportional-integral-derivative (PID) controller is the most commonly used types of compensation method in digitally controlled SMPCs [35, 36]. Finally, the DPWM generates the pulse-width-modulated control signal $c(t)$ to the gate drive, where its duty cycle is specified by the digital duty cycle $d(k)$ with constant frequency called a switching frequency [37]. The square pulses obtained from the gate drive are used to activate the power switches and run the converter. For fast and improved dynamic response, the output voltage is recommended to be sampled at least once every switching period [38].

2.7.2 *Digital Control Design Methods*

The digital controller for a PWM DC-DC converter is designed using two techniques: the design by emulation approach and the direct digital design approach. In the first method, an analogue compensator is devised in the Laplace-domain to meet certain design specifications such as settling time, overshoot, bandwidth, and then the discrete form is obtained using one of the approximation transformations such as the backward Euler, bilinear, pole-zero match. However, if the designer does not have enough information about the open-loop response of the converter, inaccurate control is designed. This lack of information is expected in PWM DC-DC converters, since the values of passive components (*L, C*) could change over time due to ageing or temperature, as well as because of unpredicted variations in the load. Furthermore, the computed discrete controller ignores the effects of sampling, quantisation, and computational delays, and therefore the overall performance of the closed loop might suffer from further degradation [20, 24].

To overcome the aforementioned sources of inaccuracy and to produce a digital controller with improved dynamic performance, a direct digital design approach is developed. In this approach, the open-loop discrete transfer function of the converter is calculated, and then all of the control design steps are performed in the z-domain according to predefined specifications in a way similar to a continuous time control design [4, 20]. In digital signal processors, the sampling and hold operation is formed by the ADC and an on-chip PWM

module, where the ADC acts as a pure sampler and the PWM holds the control signal during the sampling period and then updates it at the beginning of a new cycle. To imitate this action in the discretisation step, the ZOH transformation shown in (2.21) is the preferred approximation method to translate from the *s* to the *z* domain [20, 24, 39]. As a result, a second-order z-transfer function in the *z* for the buck converter under consideration is obtained in (2.22).

$$G_{vd}(z)=(1-z^{-1})Z\left\{\frac{G_{vd}(s)}{s}\right\} \tag{2.21}$$

$$G_{vd}=\frac{b_1z^{-1}+b_2z^{-2}}{1+a_1z^{-1}+a_2z^{-2}} \tag{2.22}$$

In (2.22) the coefficients *a* and *b* depend on elements of the Laplace transfer function formed in equation (2.18) and on the digital sampling time T_s which is usually equal to the converter switching time.

A digital controller for SMPCs which has been indirectly designed has been presented in [25]. In this approach, several discretisation methods are applied and their performance is compared in terms of some desired design specifications. The discrete controllers obtained are compared with the direct design technique. It was demonstrated that the direct design approach outperforms the indirect method in terms of peak overshoot, loop bandwidth, and phase margin. In addition, the author concluded that a backward Euler method gives better discretisation when redesigning the digital controller from the analogue one. More investigations of the selection of discretisation method have been discussed in [40].

Experimental and simulation results show that some discretisation methods cannot preserve the design specifications for the analogue controller, and hence additional manual tuning is needed. Among the discretisation methods applied, pole-zero mapping has been used to form the discrete controller [24, 41, 42]. Similarly, bilinear-transformation has been deployed to produce a discrete controller which is designed based on a pole-zero cancellation technique [29, 43, 44]. However, the frequency response obtained by the discrete controller helps the designer to select the appropriate discretisation.

Batao *et al* [4] introduced a direct digital control design approach where the discrete transfer function is extracted from real-time data by means of system identification. The proposed method has proven to be immune to common noise sources and parameter

uncertainties. Another common direct design paradigm studied in the literature is the pole-placement approach [8, 39, 45-47]. This method is extensively applied in self-tuning control strategy. El Beid *et al.* [48], presented the direct digital design control of SMPC operating in CCM. To achieve this, the discrete transfer function is first identified and then utilised directly to design a digital PID controller using a pole-assignment approach. Following the same design procedure, the Dahlin PID and Bányász/Keviczky PID controller have been developed and designed, to control a step-down DC-DC converter [51]. These two strategies compute the controller's tuning coefficients from the estimated second-order transfer function parameters. From the existing literature, it can be concluded that direct digital design methods rely entirely on the discrete transfer function of the SMPC. Therefore, in this research, a parametric system identification paradigm is presented and combined with voltage mode controller adjusted online using Bányász/Keviczky PID technique.

2.7.3 *Digital PID Controller*

In SMPC control, the PID controller is the most commonly applied compensation approach in voltage mode control. This control structure is simple, efficient, and easy to design and implement. Generally, the digital PID controller is realised as a second order linear infinite-impulse-response (IIR) filter structure. Three terms are used to formulate the PID controller in parallel form figure 2.9. These terms are named the proportional, integral, and derivative, with associated gains $K_P, K_I,$ and K_D respectively as depicted in (2.23) in a z domain [18]. Here z^{-1}indicates a unit-time delay.

$$G_{PID}(z) = \frac{d(z)}{e(z)} = K_P + \frac{K_I}{1 - z^{-1}} + K_D(1 - z^{-1}) \tag{2.23}$$

The equivalent difference equation representing the controller action is written as follows:

$$\begin{aligned} d_P(k) &= K_P e(k) \\ d_I(k) &= d_I(k-1) + K_I e(k) \\ d_D(k) &= K_D[e(k) - e(k-1)] \\ d(k) &= d_P(k) + d_I(k) + d_D(k) \end{aligned} \tag{2.24}$$

In this form, illustrated in (2.23), each gain can be adjusted individually, and hence a trial and error technique may be used and no model for the system is required. In (2.23) compensator performance and stability is shaped based on the selected values of $K_P, K_I,$and K_D. In other

words, the controller gains are tuned to meet the design specifications such as phase margin, gain margin, and loop bandwidth.

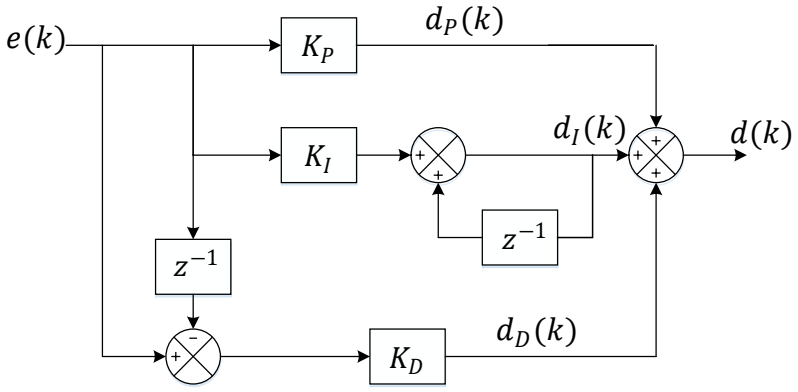


Figure 2.9 PID controller in parallel form

The proportional gain is applied directly to the loop error $e[k]$. A high value of K_P increases the loop gain and makes the controller respond instantaneously to any change in the error signal. This means that the gain of all frequency components is enlarged. Increasing the proportional gain will increase the system bandwidth and this might push the system to the verge of instability if a specific value is exceeded. Therefore, the integral term is incorporated to eliminate the steady-state error and to enhance the recovery time after any disturbance. Due to characteristics of the low-pass filter in the integral term, the controller's action becomes less affected by noise, where the high frequencies are attenuated and the low frequencies are assigned with high gain. However, the phase margin of the control loop is reduced due to the phase-lag added by the integral term, which can cause an undesirable oscillatory output response. This phase-lag is compensated by introducing the derivative term, which acts similarly to a phase-lead compensator to increase the phase-margin. Thus, the dynamic performance of the system is improved with wider stability margins. However, the derivative gain K_D amplifies the high frequency noise in the measured output. Therefore, it is recommended to limit its value to avoid potential instability in the control loop.

[49, 50].

Alongside the parallel form, the direct form is another important realisation of the PID controller (figure 2.10). Here, the PID controller is introduced as a two zeros and one pole filter [18, 29] as denoted in (2.25).

$$G_{PID}(z) = \frac{d(z)}{e(z)} = \frac{K_0 + K_1 z^{-1} + K_2 z^{-2}}{1 - z^{-1}} \tag{2.25}$$

The direct form is translated into the difference equation (2.26), which is used to implement the controller strategy on a microprocessor.

$$d(k) = d(k-1) + K_0 e(k) + K_1 e(k-1) + K_2 e(k-2) \tag{2.26}$$

$$K_0 = K_P + K_I + K_D$$

$$K_1 = -[(K_P + 2K_D)] \tag{2.27}$$

$$K_2 = K_D$$

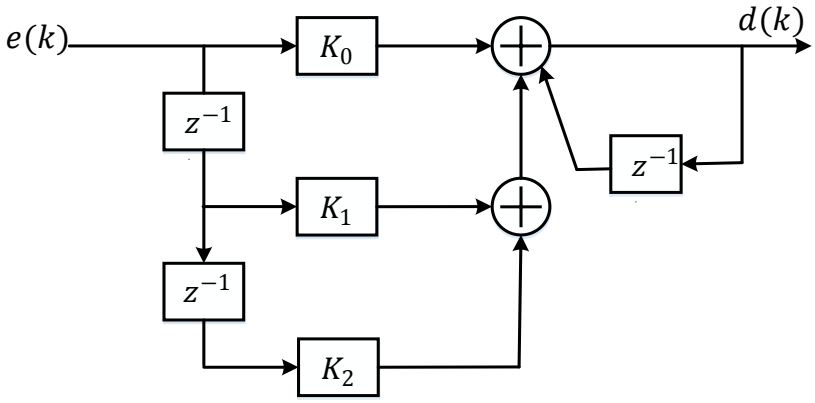


Figure 2.10 PID controller in direct form

2.8 Direct Digital Control Design for Buck SMPC using Pole Placement

2.8.1 *Overview*

This control strategy ensures that the closed-loop poles are located at defined positions in order to achieve a desired closed-loop performance [51]. As an applied direct digital design approach, the complete design of the pole placement controller is performed in the *z*-domain. The controller structure is selected to be two-poles two-zeros transfer function as in (2.28) which is the commonly applied structure in pole placement controller design [45, 51].

$$G_c(z) = \frac{d(z)}{e(z)} = \frac{q_0 + q_1 z^{-1} + q_2 z^{-2}}{(1 - z^{-1})(1 + \gamma z^{-1})} = \frac{Q(z^{-1})}{P(z^{-1})} \tag{2.28}$$

In addition, the discrete transfer function of the buck converter (2.29) is derived to form the block diagram of the closed loop system shown in figure 2.11:

$$G_{dv} = \frac{B(z^{-1})}{A(z^{-1})} = \frac{b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}} \tag{2.29}$$

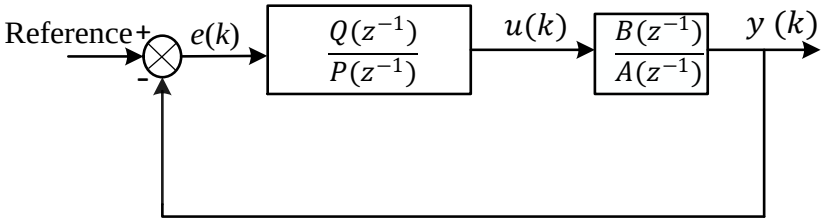


Figure 2.11 Closed loop control of the buck SMPC

Therefore, the corresponding closed-loop transfer function of the system shown in figure (2.11) is written in the following relationship:

$$G_{CL} = \frac{B(z^{-1})Q(z^{-1})}{A(z^{-1})P(z^{-1}) + B(z^{-1})Q(z^{-1})} \tag{2.30}$$

In order to obtain the desired dynamic behaviour of the closed loop system, the characteristic polynomial is found from the denominator in (2.30) [45, 52].

$$\begin{aligned} D(z) = {} & A(z^{-1})P(z^{-1}) + B(z^{-1})Q(z^{-1}) \\ & = 1 + \sum_{i=1}^{n_d} d_i z^{-i}, n_d(\text{number of poles}) \leq 4 \end{aligned} \tag{2.31}$$

The solution to the polynomial equation in (2.31) is found by calculating the controller parameters from (2.28). To do so, the characteristic polynomial of (2.31) is usually specified by a second order continuous model (2.32), where damping factor ξ and natural frequency ω_n describe the desired response of the closed loop system [53]. The characteristic polynomial is formulated as follows:

$$s^2 + 2\xi\omega_n s + {\omega_n}^2 = 0 \tag{2.32}$$

If the polynomial $D(z^{-1})$ is chosen in the form

$$D(z^{-1}) = 1 + d_1 z^{-1} + d_2 z^{-2} \tag{2.33}$$

Then the s-to-z transformation ($z = e^{sT_s}$)is used, and the coefficients d_1 and d_2 for sampling time T_s can be derived:

$$d_1 = -2e^{-\xi\omega_n T_s} \cos \omega_n T_s \sqrt{1 - \xi^2} \tag{2.34}$$

$$d_2 = e^{-2\xi\omega_n T_s}$$

If the polynomial in (2.32) is substituted into (2.30), and the equation is then written in matrix form as (2.34), the unknown PID controller coefficients are computed and presented in (2.35)

$$\begin{bmatrix} b_1 & 0 & 0 & 1 \\ b_2 & b_1 & 0 & a_1 - 1 \\ 0 & b_2 & b_1 & a_2 - a_2 \\ 0 & 0 & b_2 & -a_2 \end{bmatrix} \begin{bmatrix} q_0 \\ q_1 \\ q_2 \\ \gamma \end{bmatrix} = \begin{bmatrix} d_1 + 1 - a_1 \\ d_2 + a_1 - a_2 \\ a_2 \\ 0 \end{bmatrix} \tag{2.35}$$

$$\begin{aligned} q_0 &= \frac{1}{b_1}(d_1 + 1 - a_1 - \gamma) \\ q_1 &= \frac{a_2}{b_2} - q_2\left(\frac{b_1}{b_2} - \frac{a_1}{a_2} + 1\right) \\ q_2 &= -\frac{s_1}{r_1} \\ \gamma &= q_2\frac{b_2}{a_2} \end{aligned} \tag{2.36}$$

with

$$s_1 = a_2[(b_1 + b_2)(a_1 b_2 - a_2 b_1) + b_2(b_1 d_2 - b_2 d_1 - b_2)]$$

$$r_1 = (b_1 + b_2)(a_1 b_1 b_2 + a_2 {b_1}^2 + {b_2}^2)$$

Finally, from (2.28) the control action can be written in difference equation form as follows:

$$d(k) = [1 - \gamma]d(k-1) + \gamma d(k-2) + q_0 e(k) + q_1 e(k-1) + q_2 e(k-2) \tag{2.37}$$

2.8.2 *Simulation Results*

The synchronous buck converter presented in section (2.5) is used here to implement the pole placement control strategy. Following the design steps illustrated in the previous section, the discrete transfer function of the buck converter is computed (2.38), and the damping factor is set to 0.7 to ensure less aggressive control action with a rapid response, and the closed-loop natural frequency is selected to be twice that of the converter, for a faster settling time $\omega_n = 2\omega_0 = 7447$ rad/s [45, 46].

$$G_{dv} = \frac{0.2259z^{-1} + 0.1118z^{-2}}{1 - 1.915z^{-1} + 0.949z^{-2}} \tag{2.38}$$

The PID coefficients are determined by inserting the obtained results from (2.38) and (2.34) in (2.36), that results the control action given by:

$$d(k) = 0.1518d(k-1) + 0.8482d(k-2) + 5.0848e(k) - 8.2965e(k-1) + 3.5250e(k-2) \quad (2.39)$$

To investigate the stability of the closed-loop system, the loop transfer function frequency response $L(z) = G_c(z)\, G_{dV}(z)$ is illustrated in figure 2.12, the bode plot shows that the gain margin is 8.83 dB, and the phase margin is 39.6 degree. The designed PID controller is implemented to regulate the output voltage at 3.3 V. Further investigation has been carried out to examine the transient characteristics of the closed-loop system when a periodic load change between 5 Ω and 2.5 Ω is applied. The results shown in figure 2.13 illustrate that small overshoot and undershoot are observed when a step change in load current is experienced. Furthermore, quick recovery to the reference value is achieved and the maximum overshoot is restricted to less than 5% of the desired output voltage, which demonstrates the successful design of the PID controller using the pole placement approach.

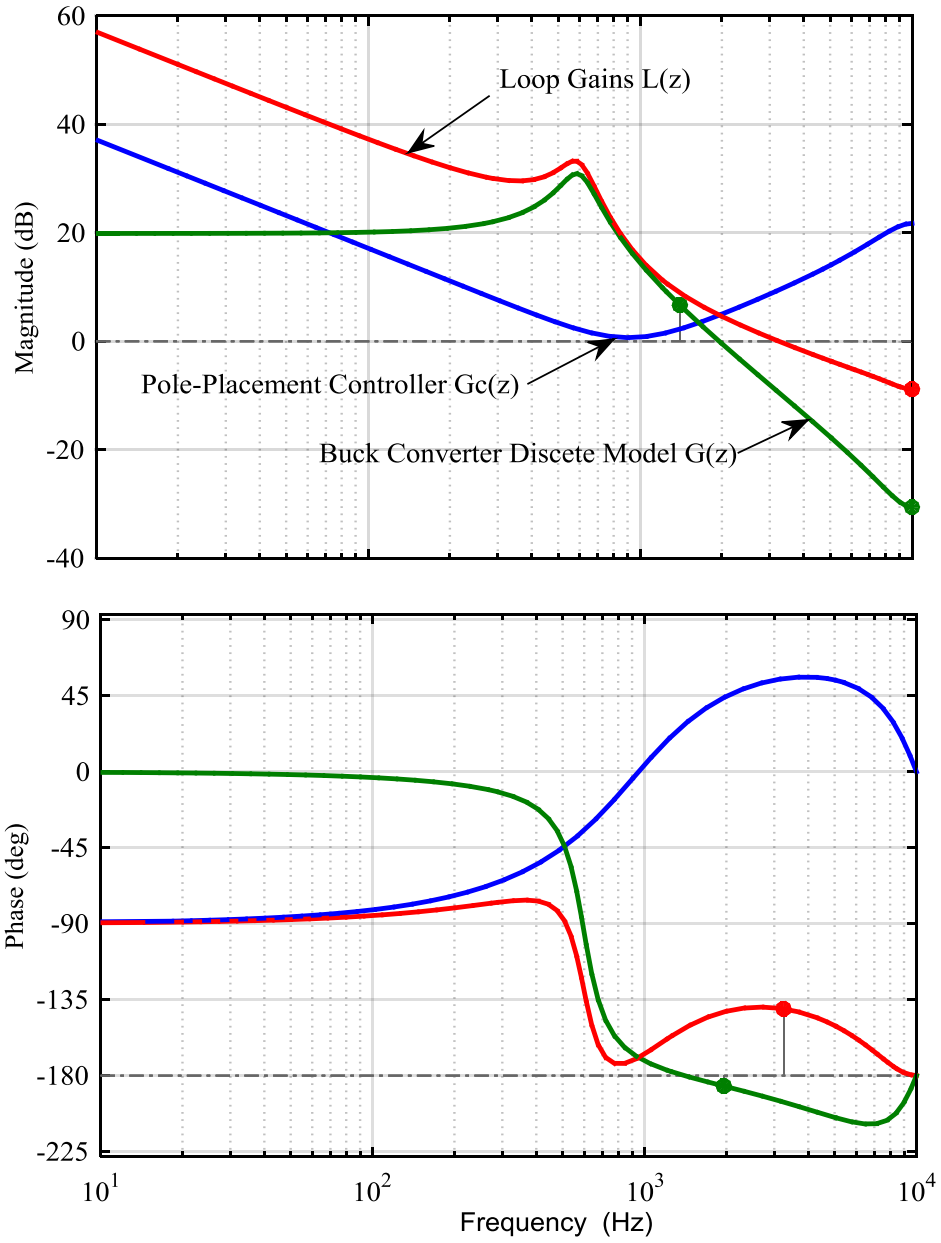


Figure 2.12 Frequency response of the compensated and uncompensated DC-DC buck converter

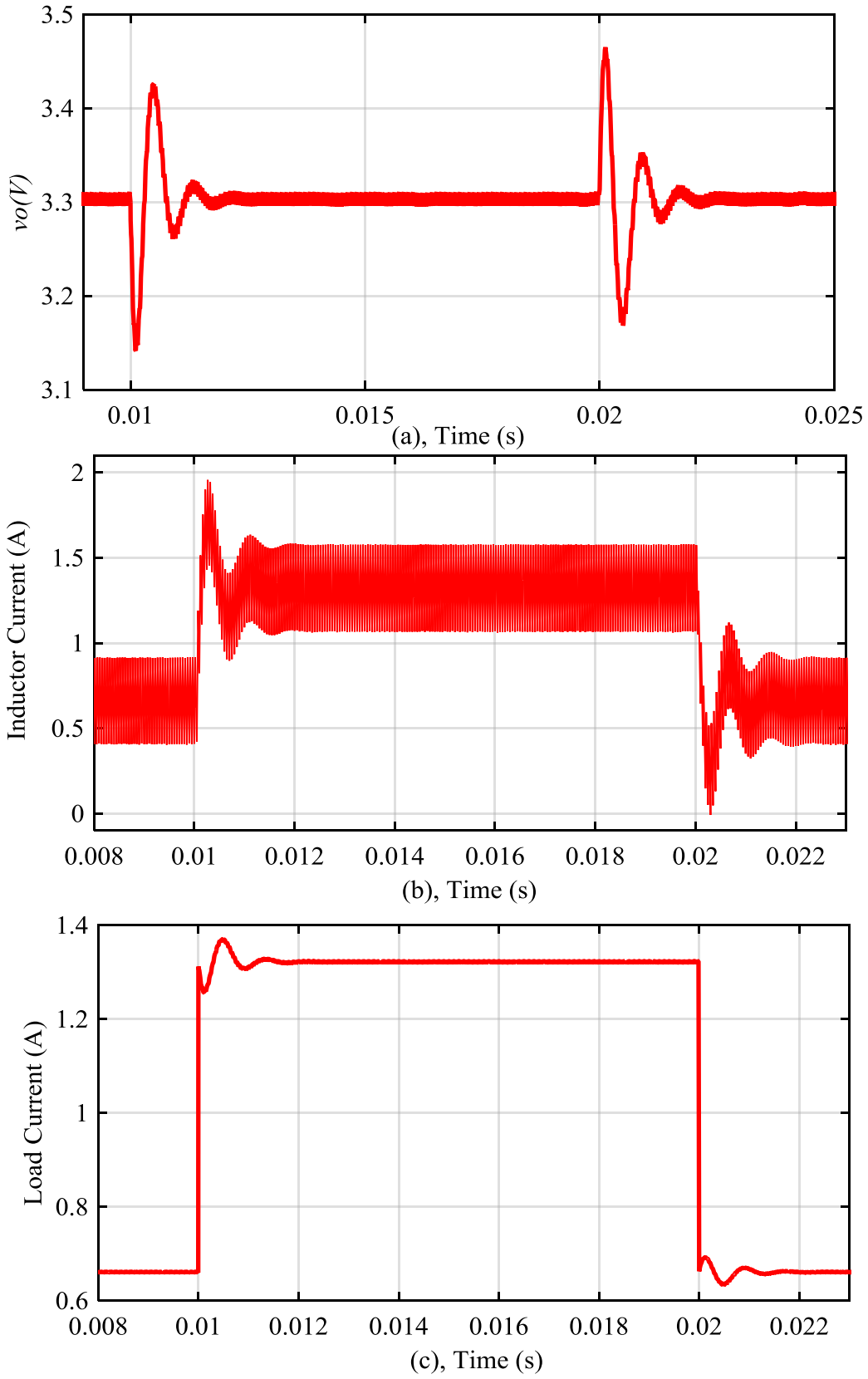


Figure 2.13 Load transient response of the pole-placement controller during 50% step load change between 5 Ω and 2.5 Ω every 10 ms: a. output voltage; b. inductor current; c. load current

The robustness of the designed controller has been tested under significant load change, which is a common scenario in DC-DC converters. To show this, a step-load change between 5 Ω and 1 Ω is repeatedly applied every 10 ms. Figure 2.14 illustrates the transient response of the output voltage, the inductor current, and the output current. According to the observed waveforms, the designed controller provides a stable closed-loop response with a clear overshoot and voltage drops as a result of the applied load step. Therefore, the stability of the closed loop is guranteed under signifcant load change, which will be applied during system identification procedure in the forthcoming chapters.

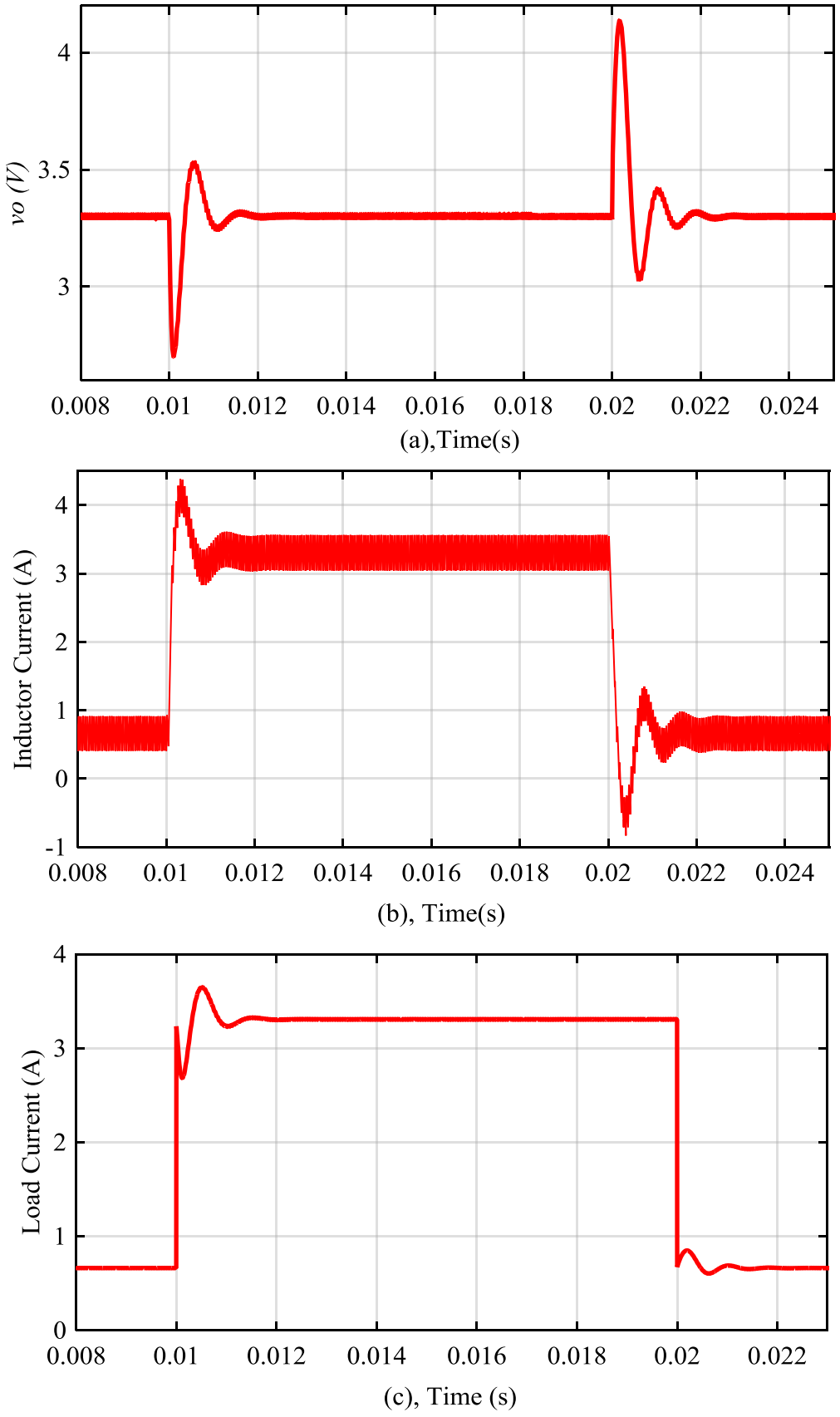


Figure 2.14 Pole-placement response during 80% load change between 5 Ω and 1 Ω every 10 ms, a: output voltage, b: inductor current, c: load current

2.9 Chapter Summary

This chapter has presented the DC-DC power converter topology, modelling and control. Due to its simple structure, the step-down circuit topology has been selected in this research as an example of a commonly used SMPC. In this chapter, a general overview of the application considered is provided in terms of operation structure, and components used. The latter is considered carefully in the field of system identification as a good knowledge of the component values can significantly contribute towards developing a robust controller and an effective condition monitoring scheme. In terms of control design, this chapter introduced the state-space average model as a cornerstone in modelling DC-DC converters. This step highlighted the derivation of the control to output transfer function for feedback control design. Once the system model is obtained, the appropriate control design method is selected. In this chapter, digital realisation of a voltage mode controller is illustrated and the two fundamental design methods are introduced.

In system identification, the system model used is usually in discrete form; therefore, a well-known direct digital design approach based on the pole assignment technique is introduced. This method utilises the discrete transfer function to design the controller. The obtained controller is implemented and tested in Matlab/Simulink to investigate its dynamic performance in response to parameter variations such as abrupt load changes. According to the results, the selected direct design method is suitable for regulating the output voltage of the converter under significant load variations. This shows the usefulness of using the discrete transfer function of the converter in controller design without the need to design an analogue controller following the classical design process. However, the discrete transfer function is required to be known in advance. This can be provided by means of prior knowledge or can be estimated while the system evolves using identification techniques. Based on the derived SSA model and the discrete transfer function obtained, a parametric identification process can be established to estimate the transfer function parameters and hence design a digital PID controller using only the information provided by the identification procedure. This is the focus of the next Chapter.

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Chapter 3 System Identification for DC-DC Converter

3.1 Introduction

As introduced in Chapter 2, knowing the model and the parameters of the DC-DC buck converter is essential to design a robust digital controller. While the model structure can be obtained using some well-known physical approaches, the parameters of this model need to be known accurately before the controller is designed. This can be achieved by means of system identification. Therefore, it is necessary to introduce this topic generally in terms of the approaches available and the steps required to use system identification efficiently for control design purposes. Recently, system identification has been used in SMPC applications for control and condition monitoring. In this chapter, an overview of the main two categories of system identification is introduced with a focus on recent research applied to SMPC. In addition, the identification procedures are described and the advantages and disadvantages of each method are highlighted. The chapter concludes by considering the use of parameter estimation techniques in the digital self-tuning control design of DC-DC SMPC applications.

3.2 System Identification Procedure

The term system identification can be defined as the determination of a mathematical model of a system from measured input and output data [54]. This technique has been widely applied in different scientific fields such as medicine, biology, aviation, and automatic control. In the area of control, system identification is employed to construct self-tuning and adaptive controllers, especially for time-varying applications [55]. Typically;

i) an experiment is conducted via injecting an enriched frequency input signal to the plant and measuring the system response.
ii) choosing or estimating the model structure using a priori knowledge;
iii) applying an identification algorithm to adjust the parameters of the selected model structure to the measured data;
iv) model validation to accept or reject the identified model (figure 3.1) [6, 56].

Among these steps, selecting the model structure is a prerequisite and can be very challenging. There are two types of modelling techniques, black-box or a posteriori modelling, and grey-box or priori modelling. In the latter approach, the model is constructed based on physical laws which describe the system dynamics, and this yields a mathematical model (state-space, transfer function, etc.) containing some unknown parameters which need to be estimated. On the other hand, in the black-box model, no previous knowledge of the system is incorporated and the model is built to describe the effect of the inputs on the outputs, which makes it suitable for representing a large class of systems [57, 58].

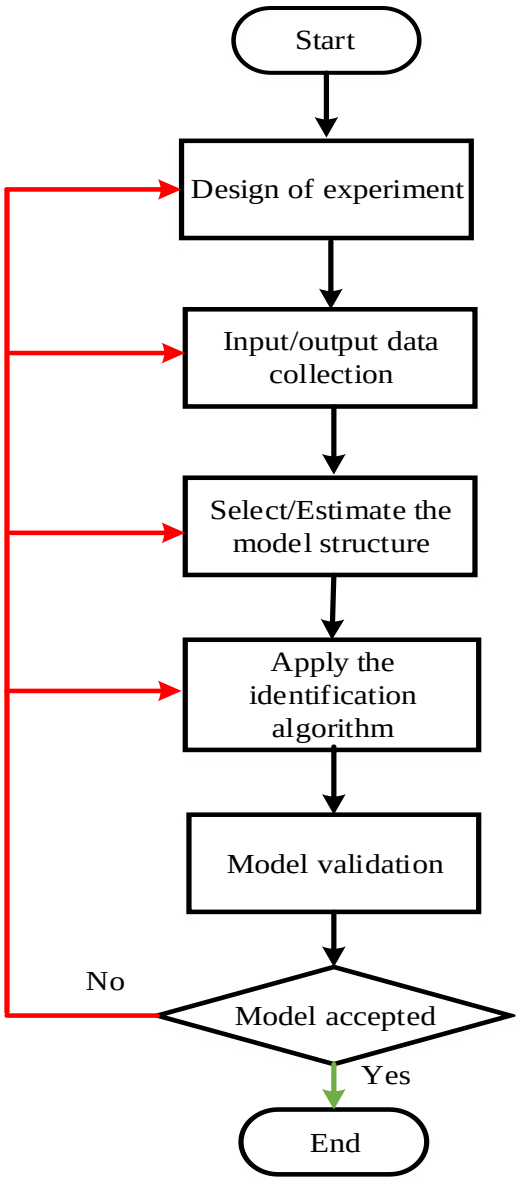


Figure 3.1 Flowchart of system identification

Following the model structure selection, the identification algorithm has to be specified. This algorithm fits the selected model to the observed data by minimising the error between the observed output and the model output. The most common identification method employed in this step is the prediction-error approach. Afterwards, the identified model must be validated to investigate the behaviour of the model with respect to a priori knowledge, the intended purpose of using the model, and the experimental data. Different methods have been used to carry out the validation step, such as residual analysis, model prediction, and simulation. If an inadequate model is obtained, the identification procedure must be repeated using another method or selecting a different model structure [56].

3.3 Implementation Methods of System Identification

In practice, the aforementioned identification procedure can be implemented on-line or off-line. The off-line method is commonly used when modelling highly complicated systems, and here the experimental data is collected and stored in memory. Following this, a sequence of post-processing and applying the identification algorithm is performed on a PC to produce an acceptable model. In contrast, on-line schemes typically use recursive estimation methods where the model parameters are updated every time a new sample becomes available, which makes it well suited for real-time applications. Therefore, on-line schemes are often utilised in adaptive control design where time-varying regulators are implemented to cope with parameter variations during operation [59]. In SMPC applications, the identification results can be tables, and curves if no physical modelling is needed, which provide useful information about the system such as the damping factor, natural frequency, time delay, and time constants. If physical modelling is involved, the identification results can be a transfer function or state-space model.

3.4 System Identification Techniques

The linear model of a system can be described in terms of frequency response, impulse response, or transfer function. In order to obtain one of these descriptions, the relevant identification method must be applied. Generally, there are two common methods widely used to estimate a linear model of the system, and these are known as non-parametric and parametric techniques [55]. Typically, an excitation signal is injected to the system, and the subsequent response is recorded and analysed to estimate the linear model.

3.4.1 *Non-parametric System Identification*

According to the input stimulus type, non-parametric techniques are divided into time domain methods and frequency domain methods. The time domain methods include impulse response, step response, and correlation analysis. In the frequency domain group, the main methods applied are Fourier analysis, spectrum analysis, sine-wave testing, and correlation analysis in the frequency domain [57]. In those techniques, only the data sets are employed without any prior knowledge of the model structure.

However, lack of accuracy, high sensitivity to noise, and the large amount of data required are the main disadvantages of non-parametric identification techniques [20]. In addition, there are some practical limitations of some non-parametric identification methods. For instance, in the case of the impulse response test, a large impulse amplitude could cause nonlinear behaviour in the system or even damage to the hardware, whereas a small amplitude requires low noise levels to excite the system, which is not the case in real-time applications. Likewise, in the sine-wave testing approach, a wide range of frequencies need to be applied at the input to accomplish accurate estimation of the frequency response. This means that long data sequences need to be processed, accompanied by increased noise sensitivity [57]. To mitigate the noise issue, correlation analysis is used in both the time and frequency domain methods [60]. In time domain methods, this approach is employed to determine an estimation of the impulse response. Consider a linear time invariant sampled system defined by the following equation [61]:

$$y(k) = \sum_{n=1}^{\infty} u(k-n)h(n) + v(k) \tag{3.1}$$

where $u(k)$ is the sampled stimulus signal, $y\ (k)$ is the sampled response signal, $h(n)$ is the discrete-time impulse response of the system being identified, and $v(k)$ represents the disturbance signal. Assuming the input signal $u(k)$ is white noise with zero mean statistically independent of the disturbance $v(k)$ and uncorrelated with the output $u\ (k)$, the cross-correlation of the input signal u(k) to the output signal $y(k)$ can be given by:

$$R_{uy}(m) = \sum_{k=1}^{\infty} u(k)\, y(k+m) = \sum_{k=1}^{\infty} h(n)\, R_{uu}(\mathrm{m}-k) + R_{uv}\,(m) \tag{3.2}$$

In (3.2), R_{uy} denotes the cross-correlation function of the stimulus signal to the response signal, R_{uv} is the input to the disturbance cross-correlation, and R_{uu} is the autocorrelation of the input signal [60]. According to the previous assumption, the autocorrelation of the white noise input signal $R_{uu}(m)$ is an ideal delta function $\delta(m)$ and the cross-correlation function $R_{uv}(m) = 0$.Thus, equation (3.2) can be simplified to define the discrete impulse response as the cross correlation function of the input signal to the output signal $R_{uy}(m)$ [62] :

$$R_{uy}(m) = h(m) \tag{3.3}$$

Furthermore, the open loop transfer function of the system in the frequency domain $H(j\omega)$ is obtained by applying the discrete Fourier transform (DFT) to the discrete impulse response (3.4) [60, 62] :

$$R_{uy}(m) \xrightarrow{DFT} H(j\omega) \tag{3.4}$$

From a practical standpoint, it is convenient to approximate the white noise input with a pseudo-random binary sequence (PRBS) perturbations generated using a shift register with feedback [61]. Despite the noise immunity demonstrated by correlation-based identification, the assumption of uncorrelated input and output signals is not satisfied in closed-loop applications due to the presence of a feedback signal [63]. Therefore, the correlation analysis is usually accomplished in the open loop to verify the predefined assumptions.

An advantage of non-parametric system identification approaches is that one can provide useful information about the system without knowing its real parameters. Accordingly, an appropriate controller is designed based on some frequency response specifications, such as loop bandwidth and margin stabilities [31]. Classically, this methodology is employed to obtain continuous time parametric models (transfer function), and their corresponding discrete time models using a discretisation method with known sampling frequency [64]. However, the transformations from the s-to-z domains and quantisation error can degrade the accuracy of model deduced [39]. Consequently, the purpose of the identification process is strongly affected. In SMPC applications, the intention behind the identification procedure can be to design and tune a digital controller, or for health monitoring issues. In this case, inaccuracy in the estimated model might lead to unstable response or inappropriate decisions taken to replace or keep passive or active components in the circuit [65].

3.4.2 *Parametric System Identification*

In this identification technique, the model strcuture is defined in advance, and the identification process directly computes the system parameters [39]. As in non-parametric methods, an appropriate excitation signal is required to cover the bandwidth of the system to be identified [66]. The estimated parameters can be the coefficients of a system difference equation, transfer function, or state-space matrix. Thus, the number of poles and zeros are specified in addition to the system order based on physical laws describing the system dynamics. This prior knowledge about the system can lead to more accurate estimation than with non-parametric methods [57, 66].

For instance, by applying Kirchhoff's current and voltage laws to the DC-DC buck converter considered in this work, the differential equations, state space, and converter transfer function are obtained as expressed in (2.2-2.17), and hence the discrete time model in (2.21). The estimated model can be utilised in simulation packages such as MATLAB/SIMULINK to obtain the non-parametric models of the step response or frequency response type with enhanced precision compared with the direct non-parametric approaches discussed in the previous section. Based on the selected representation of the model structure, a suitable parametric identification algorithm is applied to estimate a limited number of mathematical parameters; for example, the prediction-error methods for transfer function estimation and subspace-based approaches implemented in state-space estimation [56].

In (single input single output) systems SISO, as is the case in DC-DC buck converters, estimating the transfer function coefficients is preferred to acquire a more compact representation of the system due to the limited number of polynomials involved in the model structure [45]. Figure 3.2 shows the principle of Prediction Error identification Methods (PEM). Here, the discrete model parameters are adjusted at each iteration cycle using a recursive parameter adaptation algorithm. This algorithm is executed on a digital computer to minimise the difference between the system output $y(k)$ and the output of the predicted model $\hat{y}(k)$, which is called the prediction error $\varepsilon(k)$ defined by the follwing equation.:

$$\varepsilon(k) = y(k) - \hat{y}(k) \tag{3.5}$$

In figure 3.2 the stimulus input signal $u(k)$ is applied to both the real system and the adjustable discrete model. Generally, this input consists of a very low level PRBS signal added to the

original system input and it can be fulfilled either in an open-loop or closed-loop identification procedure.

As the parametric identification is performed in a recursive manner, the new parameter vector $\theta(k)$ is computed throgh adding a correction term to the previous parameter vector estimation [67]. This structure is followed by all adaptation algorithms, such as the Least Mean Square (LMS), Normalised Least Mean Squares (NLMS), Recursive Least Squares (RLS), and Kalman Filter (KF)[68]. More details of the RLS and KF algorithms are presented and discussed in the next chapter. It is worth noting that, the parameter vector $\theta(k)$ is also estimated using non-recursive algorithms, some of which use the fundamental Least Squares (LS) [69].

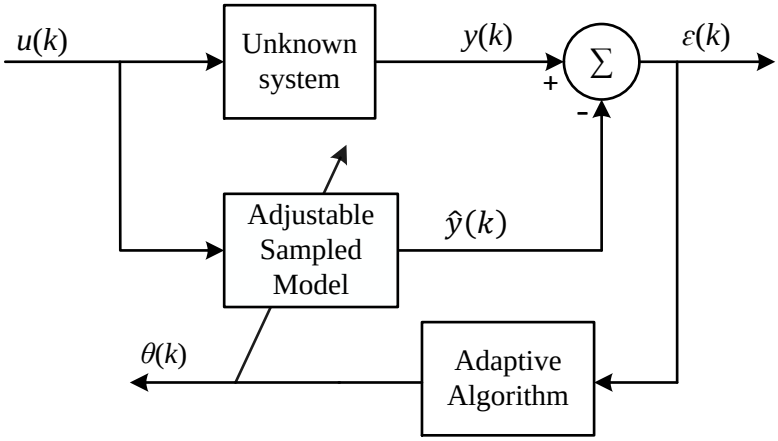


Figure 3.2. Prediction error identification method

The established recursive identification offers the advantage of continuously estimating the parameter vector as the system evolves. This yields an up-to-date parametric model which can be exploited in direct digital control design methods such as pole placement and internal model control [31, 70]. Accordingly, the error which emerges from transformation approximations from the s to the z domain are eliminated. In addition, due to the low memory requirements, recursive identification is likely to be realised in real-time on microcomputers. This feature is a key element in adaptive control where the controller coefficients or process parameters must be determined on-line [71]. Furthermore, according to the selected model structure, the disturbances can be modeled and hence their influence on the estimated parameters is reduced which grants an advantage of parametric system identification over non-parametric identification techniques [67]. However, as the dimensions of the parameter vector increases the complexity of the implemented algorithm grows accordingly, leading to higher cost for the target application. Therefore, this research introduce an efficient parametric

identification method which provides accurate estimation with lower computational cost than existing algorithms.

3.5 Linear Model Structures for PEM

In parametric identification approaches, the selection of an appropriate model structure that imitates the system dynamics is vital. Generally, a discrete system can be described using the general-linear polynomial model, as shown in figure 3.3. This general representation models the deterministic part and the stochastic part of the system as defined in equation (3.6) [57, 58]:

$$y(k) = G(z)u(k) + H(z)e(k) \tag{3.6}$$

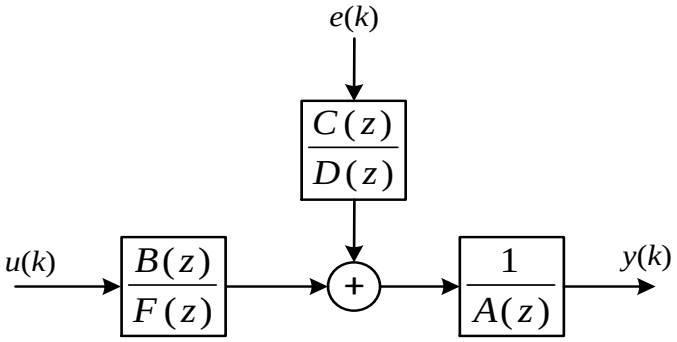


Figure 3.3 General-Linear Polynomial Model

where $y(k)$ and $u(k)$ are the sampled output and input respectively $G(z)$ is the discrete transfer function of the undisturbed system specifying the relationship between the input and the output, $H(z)$ is the stochastic behaviour of the noise that describes the impact of random noise on the system output, and $e(k)$ is assumed white noise with zero mean system disturbance. In the general model structure, the rational polynomials $G(z)$ and $H(z)$ can be expressed as following:

$$\begin{aligned} G(z) &= \frac{B(z)}{A(z)F(z)} \\ H(z) &= \frac{C(z)}{A(z)D(z)} \end{aligned} \tag{3.7}$$

where the polynomials $A(z)$, $B(z)$, $C(z)$, $D(z)$, and $F(z)$ are defined by the following equations:

$$\begin{aligned} A(z) &= 1 + a_1 z^{-1} + a_2 z^{-2} + \cdots + a_{k_a} z^{-k_a} \\ B(z) &= b_0 + b_1 z^{-1} + b_2 z^{-2} + \cdots + b_{k_b-1} z^{-(k_b-1)} \\ C(z) &= 1 + c_1 z^{-1} + c_2 z^{-2} + \cdots + c_{k_c} z^{-k_c} \end{aligned} \tag{3.8}$$

$$D(z) = 1 + d_1 z^{-1} + d_2 z^{-2} + \cdots + d_{k_d} z^{-k_d}$$

$$F(z) = 1 + f_1 z^{-1} + f_2 z^{-2} + \cdots + f_{k_f} z^{-k_f}$$

In (3.8) k_a, k_b, k_c, k_d, and k_f define the order of each polynomial. Using (3.7) and the input, the output, and the noise signal, a general description of the linear-ploynomial model is given by equation (3.9):

$$A(z)y(k) = \frac{B(z)}{F(z)}u(k) + \frac{C(z)}{D(z)}e(k) \tag{3.9}$$

The general model depicted in figure (3.3) can be simplified to produce several model structures. The obtained new models are created based on the relationship between the rational functions $H(z)$ and $G(z)$[57]. Figure 3.4 shows the most common and easiest model structure applied in polynomial model estimation, which is the so-called Auto Regressive eXogenous (ARX) model. In the ARX model, the polynomials $C(z), D(z)$, and $F(z)$ are set to 1, and therefore, the equation (3.9) is rewritten in explicit form as:

$$A(z)y(k) = B(z)u(k) + e(k) \tag{3.10}$$

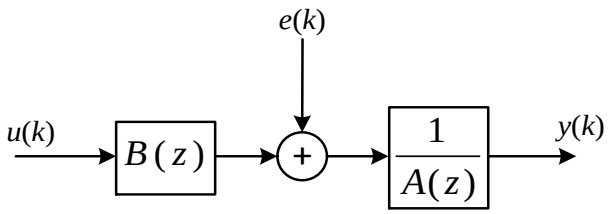


Figure 3.4 ARX model structure

In ARX model estimation, the term $e(k)$ is minimised and hence the optimum parameter vector is accomplished accurately and quickly. To achieve this, linear regression equations are solved analytically using the so-called linear LS method, which implies linearity in model parameters [6]. Therefore, the ARX model structure is considered in a variety of real-world applications especially when the model order is high [71]. Alternatively, the disturbance dynamics can be included in the model structure to form a new and more flexible model known as the Auto Regressive Moving Average exogenous (ARMAX) model as depicted in figure 3.5 [67].

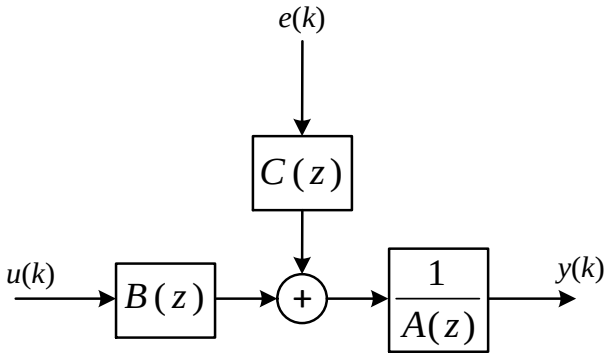


Figure 3.5 ARMAX model structure

The ARMAX model is constructed when the polynomials $D(z)$ and $F(z)$ are chosen to be $F(z)=D(z)=1$, and the incorporated disturbance $v(k)$ is characterised as a moving average of the white noise sequence $e(k)$:

$$v(k) = C(z)e(k) \tag{3.11}$$

By Substituting (3.11) in (3.9), the resulting ARMAX model is described in (3.12) [6].

$$A(z)y(k) = B(z)u(k) + C(z)e(k) \tag{3.12}$$

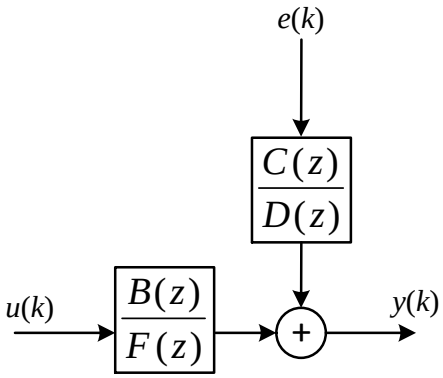


Figure 3.6 BJ model structure

Separate system dynamics and disturbance properties are represented by a Box-Jenkins (BJ) model structure as shown in figure 3.6. This type of parameterisation is preferred to model a system prone to output disturbance, such as measurement noise in real-applications [57]. Having the complete model description, the BJ equation is given by (3.13).

$$y(k) = \frac{B(z)}{F(z)}u(k) + \frac{C(z)}{D(z)}e(k) \tag{3.13}$$

In the ARMAX and BJ model structures, the numbers of parameters to be identified is increased; hence, a more complicated recursive implementation is needed. To overcome this

problem, a reduced model structure termed the Output Error (OE) model has been introduced [72]. This model structure as depicted in figure 3.7 describes only the system dynamics and no model is specified for the disturbance signal, as expressed in (3.14) [72].

$$y(k) = \frac{B(z)}{F(z)}u(k) + e(k) \tag{3.14}$$

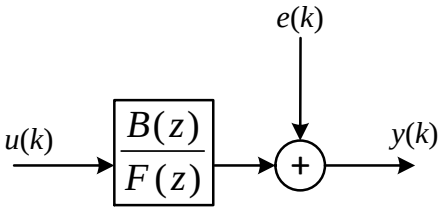


Figure 3.7 OE model structure

3.6 Parameter Estimation and Self-Tuning Control

One important motivation behind carrying out system identification is to design an appropriate controller which has the ability to control a process with time-varying parameters. This type of control scheme is considered to be a form of adaptive control strategy termed self-tuning control (STC) [45]. Figure 3.8 illustrates a block diagram of the self-tuning adaptive control system technique. Here, the depicted structure of adaptive control encompasses a recursive identification of unknown system parameters from on-line measured input/output data, and then a controller design method is implemented to compute the optimal controller based on the acquired knowledge from the estimation step [73].

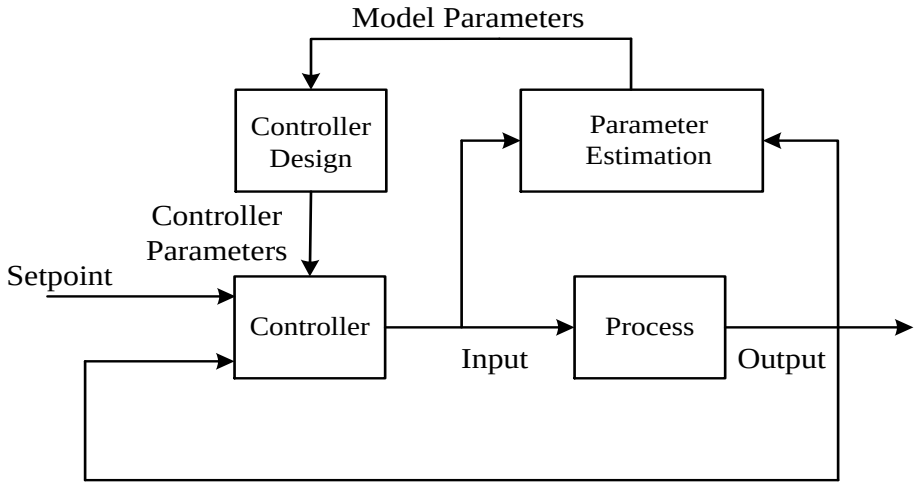


Figure 3.8 Explicit self-tuning control

The above construction is also called indirect or explicit self-tuning control, since the control relies entirely on recursive estimation to establish the controller parameters [71]. Accordingly, the identification algorithm plays a central role in this synthesis; however, the algorithm's reliability in providing accurate estimation and the computational cost are the main concerns in an explicit STC paradigm [45].

As introduced earlier in this chapter, recursive algorithms such as RLS and Extended Least Squares (ELS) can perform this task. In STC, the controller parameters are calculated in real time, therefore, the classical design methods such as frequency response or root locus do not suit this kind of control scheme. For that reason, algebraic (model-based) control has been introduced in this field to accomplish the controller design task. Pole placement, Ziegler-Nichols, dead-beat control, and minimum variance control are amongst the algebraic methods utilised in STC [71]. Here, the estimated model parameters are assumed to be correct, and that will allow the STC structure to be exploited for online fault detection or health monitoring purposes in addition to control duty. For instance, in SMPCs, the estimated discrete transfer function is used directly to design digital PID controller based on some time domain specifications such as peak overshoot, settling time, and damping factor. Also the STC is capable of monitoring and adapting to sudden changes such as load variation, which is a common scenario in SMPCs. Furthermore, the physical parameters of the DC-DC power converters can be extracted from the estimated discrete model, and hence component ageing or onset faults are detected [1, 65].

3.7 Literature Review on System Identification for SMPC

The involvement of system identification in power electronics applications has increased in recent years. This is driven by the developments in digital signal processing resources and the necessity to produce DC-DC power converters equipped with intelligent control and health monitoring schemes. Accordingly, parametric and non-parametric system identification are applied to DC-DC power converters to serve these purposes. However, the trade-off between fidelity and the complexity of the adaption algorithm is obvious; which besides, a complete real-time implementation of the self-tuning control structure for DC-DC power converters has not been fully investigated yet. In this section, a literature survey of recent

publications in this field is presented based on the technique used and the motivation behind conducting system identification procedures.

3.7.1 *Non-Parametric System Identification Methods for DC-DC Converters*

As introduced earlier in this chapter, the non-parametric system identification approach is simple and easy to apply; furthermore, it does not require any model structure to be selected in advance. Therefore, the early work published in system identification for DC-DC power converters used non-parametric techniques to accomplish this task.

In [7] various non-parametric system identification methods have been introduced and tested on DC-DC forward power converter. Here, the authors investigated the performance of time-domain and frequency-domain methods, and according to the obtained results, it is necessary that the identification experiment runs for longer in order to yield reduced error and enhanced accuracy. Correlation analysis is the most common non-parametric approach applied to identify the impulse and frequency responses of digitally controlled DC-DC power converters as introduced in [4, 60, 61, 70]. To perform the cross-correlation test, the SMPC is excited by means of the PRBS signal as an approximation of white noise added to the duty cycle, in order to satisfy the assumptions made in correlation analysis. The basic correlation analysis was modified and tested experimentally on digitally controlled switching power converter by Miao *et al.*[4]. The proposed modification included, injecting multi-periods of PRBS signal added to the duty cycle, and the impulse response of the system was obtained by means of averaging the computed cross-correlation. The time-domain model was then converted to a frequency domain model via applying the Discrete Fourier Transform (DFT) to the resultant impulse response. To confirm the reliability of the identified frequency response, the identified magnitude and phase response were compared to network analyser measurements, and showed a good agreement. It is worth noting that the target converter worked in open loop during the data collection step, besides, and a long data sequence was required to compute the correlation between the control signal and the output voltage. Furthermore, the experimental data was exported to a PC and the cross-correlation analysis was performed off-line in the MATLAB/Simulink environment.

Non-parametric system identification has been utilised for converter health-monitoring purposes [74]. Applying a correlation analysis method, changes related to the frequency response were identified to indicate any faults in the converter. The effect of low-resolution

ADC was reduced by means of pre-filtering the duty cycle perturbation, hence enhancing the frequency response fidelity in detecting any degradation in stability margins. The accuracy of the identified frequency response was then further investigated and improved via techniques borrowed from the audio engineering community [66]. The proposed identification procedure started with pre-emphasising the PRBS and then post-emphasising the measured output voltage. The cross-correlation method was used here to estimate the impulse response, which was then truncated before applying DFT to obtain a smoothed frequency response. Despite the low additional cost incurred by this method, identification takes several hundred milliseconds and also the loop was opened during the identification process. Subsequently, three different techniques to improve the accuracy of the cross-correlation identification method were proposed and implemented offline [61], including windowing the measured cross-correlation correcting for a non-ideal injected PRBS spectrum and reducing the phase shift caused by ZOH by delaying output voltage sampling. Furthermore, the improved correlation approach was used to measure the feedback loop gain without even opening the feedback loop.

Siegers *et al.*[70] incorporated the improved correlation method presented previously [61], in order to establish a digital network analyser for non-parametric identification, which was then fitted to estimate a parametric model suitable for adaptive control design. To investigate the reliability of non-parametric identification in digital control design, Jun-Yan Lio *et al.*[60] proposed a design for the digital control of a DC-DC buck converter using correlation-based identification. In [62] a multiple input multiple output (MIMO) non-parametric identification technique has also been considered for the first time in a switched-mode power converter. In this methodology, the frequency response of the converter was measured by means of cross correlating several simultaneously applied PRBS signals with their corresponding measured outputs. As with the previously presented correlation-based identification, the cross-correlation analysis was performed off-line on a PC connected with a high cost measurement card NI USB-6251, also, large numbers of data points were collected at up to 327, 600 samples in order to carry out the identification procedure.

According to the existing literature, the PRBS has been the only perturbation signal used for system identification. However, switching and quantisation effects can cause nonlinearity in SMPC that will decrease the accuracy of linear model estimation. Alternatively, the use of Inverse-repeat binary sequence (IRS) has been investigated to excite the output voltage in DC-

DC power converters in order to avoid strong nonlinear distortions, and to provide more accurate approximation of the linear part [75].

Another non-parametric identification paradigm based on the sine-sweep method has been investigated in [63, 76]. A sinusoidal perturbation was injected into the system to estimate the frequency response of the power stage of DC-DC power converter using the DFT approach in [63]. Unlike in correlation-based identification, the proposed technique was performed without the need to open the feedback loop. Although the implementation was simple, the swept frequency technique necessitated long time for the identification procedure if accurate estimation was required. The same identification methodology was exploited by Davoudi *et al.*[76] to design an off-line auto-tuning process based on an identified transfer function. Similarly, the addressed design criteria for the proposed tuning approach increased the computational time up to 105 ms to complete the identification process.

The control to output transfer function of the step-down converter has since been estimated offline [77] by applying a dual-phase lock-in algorithm. Experimental and simulation verification was performed to verify the accuracy of the proposed algorithm, which showed a better estimation when compared with DFT when the time interval did not contain an integer number of sine cycles causing a spectral leakage. Again, in [78] DFT was implemented on-line on a PC connected to a DSP controlling power converter. This method was proposed as a replacement for the classical frequency response analyser for loop gain frequency response measurement. Recently, Bhardwaj *et al.*[1] have presented a software frequency response analyser (SFRA) based on the sine-sweep technique running on a low-cost microcontroller. Here, the proposed method was investigated on a synchronous bi-directional buck power converter to measure frequency response, and then the transfer function was identified to be deployed in direct digital control design or to monitor component degradation. Elsewhere, non-parametric identification based on the sine-sweep method was combined with the recursive weighted least square approach to develop ageing detection capabilities for SMPCs [65].

In addition to deploying frequency response measurements for health monitoring purposes for SMPCs, the integration of non-parametric identification in auto-tuning control design is another possibility which has attracted more researchers in this field. For instance, the feasibility of utilising identification results to design an adaptive controller was introduced by Miao *et al.*[79]. In this work, an efficient and rapid hardware implementation of cross-correlation analysis was achieved using the Walsh-Hadamard Transformation (WHT)

algorithm and verified on a field programmable gate array (FPGA). The Xilinx Virtex-II FPGA was used as a digital controller PRBS generator, and data collection and identification processing unit. After this study, a discrete transfer function of DC-DC converter was estimated in two stages [4]. Here, the frequency response was identified experimentally first, and then the least logarithmic squares is used to obtain the parametric model from converted time domain data. To validate the identification results, a direct digital controller was designed offline and implemented experimentally on an Xilinx Vertix-II FPGA based on the discrete transfer function. High performance closed-loop dynamic voltage regulation was acheived when the converter was subjected to a step load change.

Adopting the same identification algorithm, Shirazi *et al.*[35] proposed an on-line frequency response identification to be used to construct an auto tuning PID controller for SMPC. The proposed algorithm was implemented on a Xilinx Virtex-IV FPGA, and demonstrated by application to different power converter topologies. Even with the high sampling frequency, the identification and tuning process took 350 ms to complete. A digital network analyser technique has been combined with a parametric identification method and used to design an adaptive controller of a power converter in [80]. The controller was synthesised based on the concept of internal model control, and a step-load change is applied to verify the robustness of the proposed an adaptive controller. However, this concept was demonstrated only in simulation and no experimental verification was established. Furthermore, the model-fitting procedure was conducted offline. In the most recent work in this field by Congiu *et al.*[81], a non-parametric system identification method using the power spectrum density (PSD) computation was introduced and validated on a digitally controlled buck converter. The resonant frequency and the zero frequency were both identified to characterise the control to output transfer function, and based on their values a set of PID gains were selected from a pre computed look up table to regulate the system dynamics. The proposed method was verified experimentally on a high cost Virtex6 FPGA using a VHDL-MATLAB cosimulation model.

It can be concluded that the non-parametric system identification approach assumes that the converter is in steady state operation. In addition, the majority of the methods proposed so far perform system identification while the loop is open to inject the excitation signal. Furthermore, the computational cost has not been considered as a main concern for real-time implementation, and therefore employing this type of estimation algorithm is still limited in the

product development phase and it has not been exploited in on-line implementation. Importantly, very few of the existing non-parametric system identification techniques have been developed to work on-line for self-tuning purposes.

3.7.2 *Parametric Estimation Techniques for SMPC*

Various types of parametric identification methods have been developed and extensively analysed for DC-DC power converters [3, 20, 76]. According to the literature, the conventional LS [10, 39, 82] and its recursive version, the RLS [1, 3, 83], are the most commonly applied algorithms to perform parametric identification for , analysis, control and condition monitoring purposes in SMPCs.

Alonge *et al.*[82] presented a nonlinear modelling paradigm for DC-DC converters using the Hammerstein mathematical model. The described model structure is divided into a second order linear time-invariant ARX model and a nonlinear static characteristic model. Here, the experimental data obtained is exported to the MATLAB environment to compute the transfer function parameters for the second order ARX model using the basic LS algorithm off-line. Although an accurate model is obtained in this approach, it is not suitable for real-time operation due to the complexity stemming from two steps in the identification process. Meanwhile, on-line and off-line parametric identification methods based on iterative least squares, have been demonstrated in an open-loop PWM DC-DC converter [39]. Here, a 5% step change in the duty cycle was applied to excite the system. This yielded a discrete transfer function which can be easily exploited in direct digital control design. However, due to the step change in the duty cycle, a 1 V deviation in the output voltage occurred, and this amount of overshoot is undesirable in some sensitive applications. Furthermore, the on-line implementation on TMS320F2407-DSP took 120 ms to be accomplished for a sampling frequency of 50 kHz. Again, the standard LS algorithm has been adopted, to estimate a black box model of the DC-DC converter [84]. Here, the step load change was used as a stimulus signal to excite the dynamic response of a Texas Instruments PTN78020WAZ switching converter. The captured step response was then utilised by two identification approaches to estimate the transfer function of the OE model based on a parametric LS algorithm, using a step response analysis. However, the identification step is composed of two off-line methods, which implies the suitability of this configuration for simulation work rather than real-time implementation.

The recursive parameter estimation of a SMPC was introduced for the first time by Pitel and Krein [83]. In this work, the conventional RLS was reviewed and experimentally examined on an open-loop synchronous buck converter. The authors explored three different types of perturbation signals, step impulse, white and pink noise, generated offline and uploaded to a fixed-point TMS320F2812-DSP. The experimental results obtained, confirmed that the classical RLS algorithm can give accurate parameter estimation for systems with fixed, or slowly varying, loads while operating at sampling frequency much lower than the switching frequency. However, the algorithm fails to track fast parameter changes. To overcome this issue, Algreer *et al*. [3] presented an RLS algorithm with a fuzzy variable forgetting factor to estimate the discrete transfer function of a step-down converter. In this work, the tracking abilities of classical RLS was enhanced, and accurate estimation was achieved during abrupt load changes before the output voltage even reached the peak overshoot value. However, the proposed approach has not been validated experimentally, and also the computational cost of fuzzy logic implementation was not considered.

Considering the computational cost of the previously mentioned RLS, a novel identification technique based on a dichotomous coordinate descent (DCD) algorithm, has been introduced [8]. According to simulation and initial experimental results, the identification algorithm demonstrates less computational complexity in comparison with conventional RLS, which makes it better suited for real-time adaptive control systems. Even though the proposed method was tested off-line, the convergence time for zero coefficients is long with a clear variation observed due to measurement noise. This effect could be higher if a real-time implementation was tested, which makes this algorithm not suitable for self-tuning controller design. In addition, the performance of the proposed algorithm was not investigated against fast parameter variations such as abrupt load changes.

The deployment of parametric identification in fault diagnosis has been introduced and examined on different topologies of switched-mode DC-DC power converters [1, 85-87]. Jin Kim *et al*.[88] proposed an ageing detection technique based on LS estimation for boost and buck-boost converters. The experimental data was exported to MATLAB to implement the identification process, and hence compute the ageing indicator using the estimated transfer function. Another use of parametric identification in fault detection for DC-DC converters has also been presented in [86]. In this work, a high-speed data acquisition card PCI9810 was used to collect the input/output measurements at a sampling frequency of 3 MHz, and the parameter

estimation algorithm was implemented on an industrial PC. Abdennadher *et al.* [87] developed the condition monitoring of electrolytic capacitors in boost converters by means of online parameter estimation using RLS with a forgetting factor. The estimated values of *C* and *ESR* were compared with the measured values, showing good agreement. The control and identification algorithms were both implemented on a fixed-point TMS320F2812-DSP, which indicated that the parametric identification approach can be realised in real-time for fault diagnosis and control in DC-DC converters. However, the proposed method is limited to identifying capacitor faults and cannot be generalised to other faults.

Li and Low [49] proposed a new scheme to deal with different fault scenarios in DC-DC power converters. The discrete transfer function of DC-DC buck converter is firstly estimated via RLS, then the values of actual circuit components such as output capacitance, inductors, and equivalent series resistance are retrieved using the ZOH discretisation method. This method has been experimentally validated [1, 85] on digitally controlled DC-DC buck converters. Here, the DSP TMS320F28335 was used to generate a PRBS and to realise digital PI control. Afterwards, the output voltage and the duty cycle are both sampled and transmitted to MATLAB to run the identification and mapping scheme off-line. Form the simulation and experimental results obtained based on RLS, it can be seen that the accuracy of the estimated transfer function coefficients is degraded due to measurement noise. To overcome this negative impact, another off-line parameter estimation approach using the Biogeography-Based Optimization (BBO) was proposed [1]. Due to the low sampling rate used in this approach, the estimation results took around 100 ms to converge to the final values. In addition, as the state-space model was considered for the model structure, the BBO has a considerably higher computational cost than the classical RLS. Therefore, this method has restricted application and it is appropriate for off-line identification rather than real-time parameter estimation.

To fully take the advantage of system identification results, the self-tuned adaptive controller is required to be designed on-line. This sort of implementation has been demonstrated in simulation [48, 89] and with experimental validation of the proposed combination in [90]. Indirect adaptive controller design was introduced by El Beid *et al.* [48], using recursive least squares with a forgetting factor in on-line identification. Then, the control was designed based on pole placement strategy. A repetitive load change was applied to investigate the robustness of the proposed method. However, the simulation results show only the estimation in steady state, while the accuracy of the estimated transfer function during abrupt load changes was not

investigated. Meanwhile, two digital self-tuned discrete controllers have been developed and designed [89], to control a step-down DC-DC converter which also used recursive least squares with a forgetting factor for the system identification stage. A comparative study was carried out of the Dahlin controller and the Banyasz/Keviczky PID controller for a sudden change in input voltage and/or load variation, and the simulation results indicated that the self-tuned Dahlin controller outperforms the Banyasz/Keviczky PID controller in terms of model inaccuracy and disturbance.

Elsewhere, an indirect self-tuning adaptive controller based on parametric estimation method has been introduced in [90, 91]. Here, the discrete transfer function coefficients of SMPC are estimated using Recursive Least Squares (RLS) algorithm and the controller is designed following a pole-placement method. However, the overall complexity of this combination is high due to the requirement of a high number of mathematical operations used in RLS estimation. For this reason, the sampling frequency is selected to be much lower than the switching frequency in order to realise the proposed scheme on low-cost microcontrollers. Again, a model-based controller outperformed a fixed gains PI controller designed using the frequency domain conventional method [92]. In this work, the Hammerstein approach [82] was adopted for the identification step, and the consequent robust control of a quadratic DC-DC step-up converter was designed based on an identified set of transfer functions. The fourth order ARX model was estimated by an ordinary LS algorithm, and the discrete transfer function obtained was utilised to realise the robust controller formed in a look up table. The suggested control algorithm was validated experimentally on a high cost DSPACE DS1103 board, with the possibility to be implemented on DSP or FPGA with insignificant augmentation in terms of computational burden.

3.8 Chapter Summary

This chapter has reviewed the basics of system identification, including the main categories of methods used and the steps followed to perform the identification procedure successfully. The well-known non-parametric and parametric identification approaches have been presented and discussed in detail. As the most important step in the parametric identification paradigm, the commonly applied model structures have been introduced with illustrations of their corresponding advantages and disadvantages. Full descriptions of the pre-processing techniques used are also included to explain the data preparation prior to the identification process. Different types of model validation methods have been explained, with more of these focusing on model validation based on the prediction error approach. The self-tuning adaptive control strategy is reviewed as a motivation for performing system identification.

A literature survey of recently published research on system identification for DC-DC SMPCs has been presented and classified based on the identification method applied. This survey has shown that despite the good performance achieved using the non-parametric identification methods, the implementation cost is still high as more complicated and costly embedded systems are required, which is undesirable, in particular, for small and high volume systems such as DC-DC SMPCs. Therefore, the non-parametric identification methods are mostly used during the product development phase rather than in real-time implementation. On the other hand, the RLS is the commonly applied algorithm in parametric identification approach and can be utilised to build a complete package of self-turning control in real-time. Referring to the literature, this algorithm suffers from degradation in estimation accuracy due to measurement noise, and difficulties in tracking time varying parameters. For these reasons, a new parametric identification method based on KF approach is introduced in this work for the first time in system identification of DC-DC converters to mitigate the RLS shortcomings. In addition, very few of the existing literature consider the computational complexity and the real-time implementation of system identification. Therefore, a new computationally efficient estimation algorithm based on partial update KF (PUKF) suitable for real-time implementation is proposed in this work and then embedded with the Bányász/Keviczky PID controller, in order to produce a new and computationally light self-tuning controller.

Chapter 4 Parameter Estimation of DC-DC Power Converter Using Kalman Filter Approach

4.1 Introduction

Incorporating adaptive filtering algorithms to control system design has become an area of active research over the last two decades, particularly for applications where system parameters vary over time and the controller gains need to be continually updated. This can be clearly seen in STC applications, where an adaptive filter is used in the system identification scheme. In digital signal processing, there are two primary types of digital filters, named the Finite Impulse Response (FIR) filter and Infinite Impulse Response (IIR) filter. The latter has both adaptive poles and zeros, and is also known as a poles/zeros filter; therefore, the IIR filter is preferred in modelling unknown systems with poles and zeros in the desired model such as DC-DC SMPCs. In addition to the digital filter structure, the selection of the adaptation algorithm is vital in adaptive system identification. According to the literature review, various parametric algorithms such as LS and RLS are utilised to estimate the discrete transfer function in such a way that the error between the system output and the digital filter output is minimum [93]. Unfortunately, in many of the methods discussed in the literature review, a trade-off always exists and there is no an adaptation algorithm which can provide all desirable features simultaneously. In general, there are several factors which can be considered to evaluate the overall performance of adaptive algorithms in system identification convergence such as speed, estimation accuracy, computational complexity, and numerical robustness [94].

In SMPC applications, it is very important that the adaptive filter coefficients are estimated as accurately as possible during the steady state and during abrupt changes since this will ultimately determine the closed loop controller response. Therefore, a parametric estimation algorithm which can handle the identification process efficiently is required to be implemented in real-time. For this reason, this chapter introduces a state-of-the-art Kalman Filter (KF) algorithm for real-time parameter estimation. This method is implemented here for the first time in system identification of DC-DC SMPCs.

The proposed technique has the advantage of providing an independent strategy for the adaptation of each individual parameter. Compared to existing system identification

approaches, the proposed algorithm can be readily implemented on-line and is well-suited for real-time dynamic applications. Furthermore, unlike classical RLS approaches, the effects of the excitation signal and parameter uncertainty can be factored into the proposed algorithm. This results in greater precision in parameter estimation and much faster convergence speed. In order to improve the performance of the proposed KF, a new tuning technique that allows greater freedom to tune the recursive estimation and accurately tracking time-varying parameters is also presented. This is achieved by updating the parameter vector coefficients at different rates, which is different also from other existing schemes.

4.2 Recursive Least Squares with Exponential Forgetting (ERLS)

For an assumed ARX model structure, the ordinary LS is the fundamental method used for parameter estimation in linear systems [95]. In the LS algorithm, a finite parameter vector θ is estimated in order to find the best fit between the predicted model output $\hat{y}(k)$ and the measured output $y(k)$ over a determinate number of observations, in such a way that the sum of the squared error is at a minimum (figure 4.1)[96].

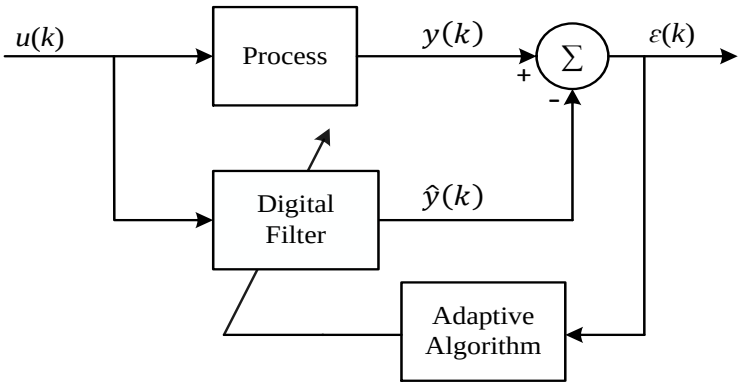


Figure 4.1 An Adaptive Filter configured for system identification

This scaler is required to be zero or small enough in order to obtain a good estimation result. Formally stated, the parameter vector θ is selected to minimise the cost function $J(\theta)$ [6]:

$$J_\theta(k) = \sum_{k=1}^{M} \varepsilon[(k)]^2 = \sum_{n=1}^{k} [y(k) - \varphi^T(k)\theta]^2 \qquad (4.1)$$

With M is the sample size of the data, an analytical solution can be found for the quadratic cost function $J_\theta(k)$ to deduce the Least Squares estimation as follows [96]:

$$\hat{\theta}_{LS} = \left[\sum_{k=1}^{M} \varphi(k)\,\varphi^T(k)\right]^{-1} \sum_{k=1}^{M} \varphi^T(k)\,y(k) \tag{4.2}$$

where:

$$y(k) = \varphi^T(k)\theta + \varepsilon(k) \tag{4.3}$$

$$\varphi(k) = [-y(k-1), \dots, -y(k-n_a),\ \ u(k-1), \dots,\ u(k-n_b)]^T \tag{4.4}$$

$$\theta = [a_1, \dots, a_{n_a}, b_1, \dots, b_{n_b}]^T \tag{4.5}$$

It can be seen in (4.2), that the linear LS algorithm performs a matrix inversion to compute the parameter vector estimate $\hat{\theta}_{LS}$ using previously stored measurements. However, if on-line estimation is considered, the fundamental LS algorithm becomes inefficient, as the size of the data batch will increase at each time step. Consequently, more memory is required to perform this operation as new observations are added to the data vector sequentially [73].

To save computational time and hence the implementation cost, the least squares estimate can be computed recursively resulting in RLS-based algorithms, which are extensively used in the STC framework [56, 71]. In this type of adaptive algorithm, the obtained estimation at time (k-1) is used to obtain the estimate at the current time (k) instead of recalculating $\hat{\theta}_{LS}$ using the entire data set [71]. The conventional RLS can be visualised as in figure 4.2 and is summarised in Table 4.1. (Appendix A shows the derivation details of the RLS algorithm using matrix inversion lemma).

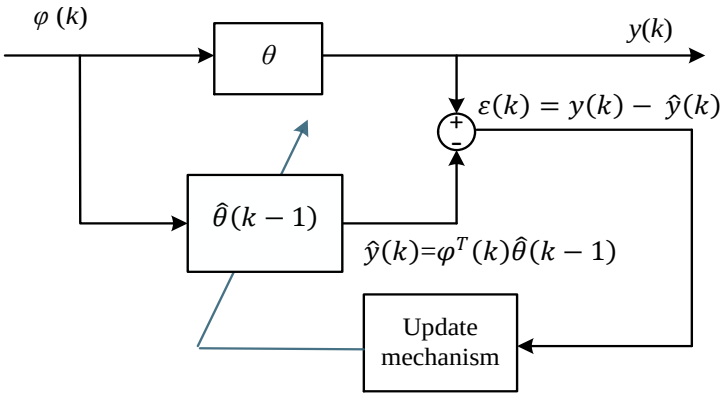


Figure 4.2 Block diagram of the RLS approach

In Table 4.1, $P(k) \in \mathrm{R}^{N\times N}$ is the error covariance matrix, $K(k) \in \mathrm{R}^{N\times 1}$ is the adaptation gain vector or Kalman gain, and N is the number of parameters to be estimated. The initial

choices of the system parameters $\hat{\theta}(0)$ and covariance matrix $P(0)$ are selected by the designer, and the role of experience and intuition is paramount. [68, 85].

Table 4.1 Classical RLS algorithm based matrix inversion lemma

Step	Formula
	$\hat{\theta} = 0, P(0) = g * I$, g >1
	For each *u(k), y(k), k* ≥ 1, do
1	$\varepsilon(k) = y(k) - \varphi^T(k)\hat{\theta}(k-1)$
2	$K(k) = \dfrac{P(k-1)\varphi(k)}{I + \varphi^T(k)P(k-1)\varphi(k)}$
3	$\hat{\theta}(k) = \hat{\theta}(k-1) + K(k)\left[y(k) - \varphi^T(k)\hat{\theta}(k-1)\right]$
4	$P(k) = [P(k-1) - K(k)\varphi^T(k)P(k-1)]$

In SMPCs, some circuit components are considered to be time-varying; for instance the effect of ageing upon the energy storage components (capacitor and inductor) or possible load variations [65, 74, 97]. In this situation, the Exponentially Weighted Recursive Least Squares (ERLS) is developed as an extension to the standard RLS, in order to capture the parameter variation. In this approach, the least squares criteria of (4.1) is replaced by the following [6, 73]:

$$J_\theta(k) = \sum_{n=1}^{k} \lambda^{k-n}[y(n) - \varphi^T(n)\theta]^2 \tag{4.6}$$

where λ is a nonnegative coefficient such that (0 << λ < 1), and this is known as the forgetting factor or discounting factor. As stated in (4.6), the most recent data is given more weight more than past data according to the performance criteria λ^{k-n}. In ERLS, the discounting factor is used to inflate the covariance matrix elements exponentially as denoted in (4.7) [93, 98]:

$$P(k) = \frac{1}{\lambda}\left[P(k-1) - \frac{P(k-1)\varphi(k)\varphi^T(k)P(k-1)}{\lambda + \varphi^T(k)P(k-1)\varphi(k)}\right] \tag{4.7}$$

Here, the appointed value of λ influences the performance of the RLS algorithm, as it affects on the algorithm's alertness in terms of the adaptation gain. In other words, if a small value of λ is selected, the tracking capability of the RLS algorithm is improved, but the estimation becomes more sensitive to noise. On the other hand, a constant value of λ very close to one will mitigate the numerical problems caused by large adaptation gain, at the expense of

poor and sluggish tracking performance for time-varying parameters [99]. To alleviate this problem, RLS algorithms with a variable forgetting factor (VFF) have been used to simultaneously enhance the adaptation capabilities and decrease the steady state misalignment [73, 98, 100]. However, most of the proposed VFF strategies involve some design constants need to be chosen using trial and error as proposed in several studies [100-102]. Moreover, the computational complexity of the adaptation mechanism is increased [99, 103]. Regardless of the method used to find the forgetting factor, the main steps of the ERLS algorithm can be summarised as in Table 4.2.

Table 4.2 ERLS algorithm for time varying parameters

Step	Formula
	$\hat{\theta}(0) = 0, P(0) = g * I$, g >1, 0 << λ < 1
	For each *u(k), y(k),* $k \geq 1$, do
1	$\varepsilon(k) = y(k) - \varphi^T(k)\hat{\theta}(k-1)$
2	$K(k) = \dfrac{P(k-1)\varphi(k)}{\lambda + \varphi^T(k)P(k-1)\varphi(k)}$
3	$\hat{\theta}(k) = \hat{\theta}(k-1) + K(k)\left[y(k) - \varphi^T(k)\hat{\theta}(k-1)\right]$
4	$P(k) = \dfrac{1}{\lambda}[P(k-1) - K(k)\varphi^T(k)P(k-1)]$

4.3 The Disadvantages of ERLS Algorithm

According to the operational steps in Table 4.2, the ERLS technique applies equal weight to all parameters during the estimation process. As a result, if the rate of variation of one of the estimated parameters is greater than those of the other parameters, the same adaptation gain correction is applied to all parameters, which greatly affects the estimator output [104]. The estimation of coefficients with small values will suffer from slow convergence speed and higher estimation error.

In practice, the measurement noise may increase this deviation, which impacts on the reliability of the estimation results when used in fault detection applications, or controller design on-line. This scenario is illustrated in the parameter estimation of DC-DC SMPC, where sluggish convergence of the zero coefficients is observed and their final values are strongly affected by measurement noise [1, 8]. Another drawback of the ERLS implementation is the

requirement of superimposing the input signal with a frequency-rich signal (such as those generated by a Pseudo Random Binary Sequence: PRBS) to enhance the estimation accuracy and prevent estimator wind-up due to an exponential growth in the adaptation gain matrix [104]. This necessitates keeping the output voltage perturbed for long periods or resetting the estimator periodically, which can lead to some abrupt changes not being observed. To overcome this, the error covariance matrix can be updated using a different approach to add more freedom to the adaptive algorithm when calculating the adaption gain. Therefore, the KF is introduced in the following section as the first contribution of this work.

4.4 Kalman Filter Algorithm Configured for Parameter Estimation

The Kalman Filter is a recursive method widely used to estimate unmeasured states in a linear dynamic system [68, 105]. In some cases, the estimated state vector is expanded to include the parameter vector as an additional state [106, 107]. To provide the necessary clarification, one can consider the stochastic component in the state-space model of the system in terms of the transition and the observation equations in discrete form for a time-varying case [108, 109]:

$$x(k+1) = Fx(k) + w(k) \tag{4.8}$$

$$y(k) = Hx(k) + v(k) \tag{4.9}$$

Here, $x(k) \in \mathrm{R}^{N\times 1}$ is the state vector, $F \in \mathrm{R}^{N\times N}$ is the state transition matrix, $y(k)$ represents the measured output, k is the time index, and $H \in \mathrm{R}^{1\times N}$ is the output vector. The process noise $w(k)$ and the measurement error $v(k)$ are uncorrelated random vectors with zero-means and their associated covariance matrices are given by:

$$\begin{aligned} E\left[w_i {w_j}^T\right] &= S\delta_{ij} \\ E\left[v_i {v_j}^T\right] &= R\delta_{ij} \\ E\left[w_i {v_j}^T\right] &= 0 \end{aligned} \tag{4.10}$$

where; $E[.,.]$ symbolises the expectation operator and δ_{ij} is the Kronecker delta function. In this process, the Kalman filter approach seeks the optimal estimate of the state vector $x(k)$, denoted by $\hat{x}(k)$, using all the available measurements $y(k)$ [68]. The is achieved via minimising the mean squared error function, which is equivalent to:

$$P(k) = E[\varepsilon(k)\varepsilon^T(k)] = E\left[\big(x(k)-\hat{x}(k)\big)\big(x(k)-\hat{x}(k)\big)^T\right] \tag{4.11}$$

where; $P(k)$ is an (N×N) error covariance matrix. The KF for state estimation can be configured as a cyclic two-state recursive algorithm, with the first step as the time update or prediction step and the second step for measurement updating or correction. These two phases represent the basis for the Kalman filter algorithm, which bears a resemblance to a predictor-corrector estimation algorithm [95].

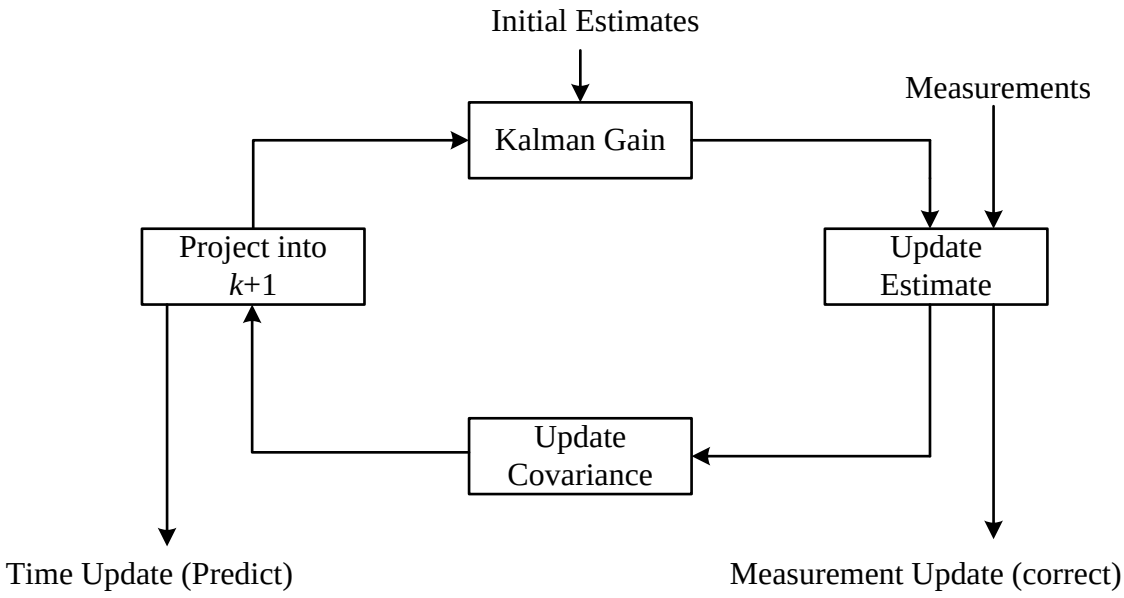


Figure 4.3 Kalman filtering structure [110]

As illustrated in figure 4.3, the update equation for the new estimate can be written by combining the prior estimate (initial estimate) of $\hat{x}(k)$ denoted by $\hat{x}'(k)$ or $\hat{x}(k-1)$ and the observation data as follows [111]:

$$\hat{x}(k) = \hat{x}'(k) + K(k)[\, y(k) - H\hat{x}'(k)] \tag{4.12}$$

where; $K(k)$ is the Kalman gain which will be derived shortly, and the term $y(k) - H\hat{x}'(k)$ is recognised as the innovation or measurement residual, this term can be rewritten by substitution of (4.9) into (4.12) gives [110]:

$$\hat{x}(k) = \hat{x}'(k) + K(k)[\, Hx(k) + v(k) - H\hat{x}'(k)] \tag{4.13}$$

As a result, the covariance matrix of ε (k) can then be expressed as:

$$P(k) = E\big[[(I - K(k)H)\big(x(k) - \hat{x}(k)\big) - K(k)v(k)][(I - K(k)H\big(x(k) - \hat{x}(k)\big) - K(k)v(k)]^T\big] \tag{4.14}$$

Note that the state estimation errors and process noise are uncorrelated, and therefore equation (4.14) can be simplified to result in the associated covariance given by:

$$P(k) = (I - K(k)H)E\left[\left(x(k) - \hat{x}(k)\right) - \left(x(k) - \hat{x}(k)\right)^T\right](I - K(k)H) + K(k)E[\, v(k)v^T(k)]\, K^T(k) \tag{4.15}$$

Substituting (4.10) and (4.11) into (4.14) and considering the prior estimate of $P(k)$ denoted by $P'(k)$ gives the update equation of error covariance matrix:

$$P(k) = (I - K(k)H)P'(k)(I - K(k)H)^T + K(k)RK^T(k) \tag{4.16}$$

The trace of this covariance matrix determines how good the estimate of the state variables at a given iteration is. As a result, the Kalman gain should be designed in order to minimise the trace of $P(k)$ [68]. By expanding and differentiating (4.16) with respect to $K(k)$ and setting the result equal to 0, the optimum value of the Kalman gain $K(k)$ is computed as:

$$K(k) = \frac{P'(k)H}{R + HP'(k)H^T} \tag{4.17}$$

Using the optimal gain sequence in (4.17), it is possible to reformulate the update step of the error covariance matrix $P(k)$ as follows:

$$P(k) = P'(k)[I - K(k)H] \tag{4.18}$$

After the update stage is accomplished using (4.17), (4.12), and (4.18), state projection or the prediction step into the next time interval, (k+1) is attained using:

$$\hat{x}(k+1) = F\,\hat{x}(k) \tag{4.19}$$

Using the above expression in (4.11) and the zero cross-correlation between $\varepsilon(k)$ and $v(k)$, we can write the following equation, which projects the error covariance matrix into the next time interval, (k+1):

$$\begin{aligned} P'(k+1) &= E[F\varepsilon(k)(F\varepsilon(k))^T] + E[w(k)w^T(k)] \\ &= FP(k)F^T + S(k) \end{aligned} \tag{4.20}$$

Here, $S(k)$ is the process noise covariance matrix defined in (4.10). Finally, the recursive filter for a linear stochastic system with a state-space description is completed. The salient mathematical expressions are combined and summarised in Table 4.3.

Table 4.3 Kalman filter recursive algorithm for state estimation.

Description	Formula
Kalman Gain	$K(k) = \frac{P'(k)H}{R + HP'(k)H^T}$
Update Estimate	$\hat{x}(k) = \hat{x}'(k) + K(k)[\, y(k) - H\hat{x}'(k)]$
Update Covariance	$P(k) = P'(k)[I - K(k)H]$
Project into $k+1$	$\hat{x}(k+1) = F\,\hat{x}(k)$ $P'(k+1) = FP(k)F^T + S(k)$

According to the anatomised components of the KF state estimation, a clear resemblance is observed between the recursive estimator of time-varying parameters ERLS and the KF [56, 71]. In other words, the presented sequence can be configured for parameter estimation by defining the state-space model as follows:

$$y(k) = \varphi^T(k)\hat{\theta}(k) + v(k)$$
$$\hat{\theta}(k) = \hat{\theta}(k-1) + w(k) \tag{4.21}$$

More precisely, the output vector H is simply the regression vector φ^T, and an identity matrix is assigned for the state transition matrix F, and henceforth the suitability of the Kalman filter as a parameter estimator becomes evident. In this revised form, the parameter vector θ is the entity to be estimated instead of the state x, the parameter changes are driven by the random vector $w(k)$ with covariance S, and $v(k)$ is the observation noise with variance r [68, 112]. Table 4.4 demonstrates the implementation sequence of the Kalman filter as a parameter estimator [112].

Table 4.4 Kalman filter recursive algorithm for parameter estimation

Description	Formula
Initialisation	$P(0) = g * I$, and $\hat{\theta}(0) = 0$, where I is an $N \times N$ identity matrix, g is large number, r is scaler > 0, S is diag $[S_{11}, S_{22}, .., S_{NN}]$
	Do for $k \geq 1$
Kalman Gain	$K(k) = \frac{P'(k)\varphi(k)}{r + \varphi(k)P'(k)\varphi^T(k)}$
Update Estimate	$\hat{\theta}(k) = \hat{\theta}(k-1) + K(k)\left[y(k) - \varphi^T(k)\hat{\theta}(k-1)\right]$
Update Covariance	$P(k) = P'(k)[I - K(k)\varphi^T(k)]$
Project into $k+1$	$P(k+1) = P(k) + S(k)$

As shown in Table 4.4, at the prediction step the error covariance matrix is computed by the additional inclusion of a diagonal matrix S to account for time-varying parameters. The size of the diagonal elements are conducive to the corresponding parameter variation in a random walk. Thus, the adaptation gain is adjusted for each parameter individually, and this yields more accurate estimation of all elements in the vector θ with comparable convergence times and more flexibility in tuning. In contrast to the ERLS illustrated in Table 4.2, a linear growth of the covariance matrix P is observed in the Kalman filter. This allows the estimator to work for longer periods of time without any significant output perturbations. Unquestionably, the estimator will exhibit operational alertness over the operating time. For this reason, the KF approach is considered to be excellent choice for real-time applications such as DC-DC converters where long periods of perturbation in the output voltage are highly undesirable. Since the same initialization techniques as for ERLS are followed with the KF, the process noise covariance matrix (S) and measurement noise variance (r) remain as the problematic parameters which have to be supplied by the designer using a trial and error procedure, until the desired filter output response is attained [113]. However, in real-time implementations the use of ad hoc methods is impractical. Therefore, a self-tuned KF employed in the parameter estimation of a step-down DC-DC converter is proposed and discussed in the next section.

4.5 Kalman Filter Tuning in the Parametric Identification of SMPC

The process noise covariance matrix S is the most critical tuning parameter in the KF used for state or parameter estimation, as it requires a priori knowledge of the process noise statistics and the expected parameter variations [108]. In the KF configured for parameter estimation, the tracking capability of the estimator relies entirely on the value of S, as small values in the diagonal elements indicate that only small changes are expected, producing a small adaptation gain K that can only adapt slowly. On the other hand, a large value of S leads to large values of P and thus large gains that make the estimator more sensitive to noise [114]. Therefore, several methods and approaches have been proposed to alleviate the deleterious effects related to the tuning of this matrix, in particular if a real-time implementation of the algorithm is required [109, 115].

In this work, an adaptive tuning method for process noise covariance S is introduced, and this approach was initially provided for KF-based state estimation in [116, 117]. Here, the

modified version of this tuning scheme, computes each diagonal element in the matrix *S* based on its related innovation term and Kalman gain. Therefore, individual parameters with different rates of variation can potentially be tracked more accurately. Referring to Table 4.4, in step 2 the parameter variation can be estimated from:

$$\hat{w}(k) = \hat{\theta}(k) - \hat{\theta}(k-1) = K(k)[\, y(k) - \varphi^T(k)\hat{\theta}(k)] \tag{4.22}$$

As a result, different variance estimates are obtained for each element in the vector $\hat{w}_k$ as follows:

$$\hat{S}_{ii}(k) = [\hat{w}_i(k)]^2 \tag{4.23}$$

The deduced model error covariance in (4.24) is a time-varying matrix, iteratively used to improve the tracking capability of the filter in the event of any sudden change in system parameters such as an abrupt load change in DC-DC converter.

$$\hat{S}(k) = \begin{bmatrix} [\hat{w}_1(k)]^2 & 0 & 0 & 0 \\ 0 & [\hat{w}_2(k)]^2 & 0 & 0 \\ 0 & 0 & [\hat{w}_3(k)]^2 & 0 \\ 0 & 0 & 0 & [\hat{w}_N(k)]^2 \end{bmatrix} \tag{4.24}$$

Using this matrix in updating the error covariance matrix *P*, each diagonal element in *P* will be updated according to the corresponding innovation term; hence the components of parameter vector $\hat{\theta}(k)$ will have different variance estimate due to the assigned adaptation gain. This new tuning approach overcomes the difficulties faced in ERLS in estimating small parameters from noisy real-time data and tracking the sudden changes in system parameters. Therefore, the estimation accuracy and the tracking performance can be improved significantly for all transfer function coefficients.

4.6 The Proposed Parametric Identification Scheme Using KF Approach

Following a typical identification procedure introduced in Chapter 3, the proposed parametric identification scheme can be constructed as shown in figure 4.4. Here, the system identification block is inserted alongside a digital PID controller used in the voltage mode control of a synchronous DC-DC buck converter. In this block, an adaptive system identification algorithm is performed continuously to estimate a discrete model of the buck converter system on a sample-by-sample basis. While the converter is operating, the

identification process can be enabled and disabled during the start-up of the converter, or during the steady state operation at regular set of intervals, alternatively, it can be activated if any change in the system is detected such as abrupt load change in SMPC [8, 83].

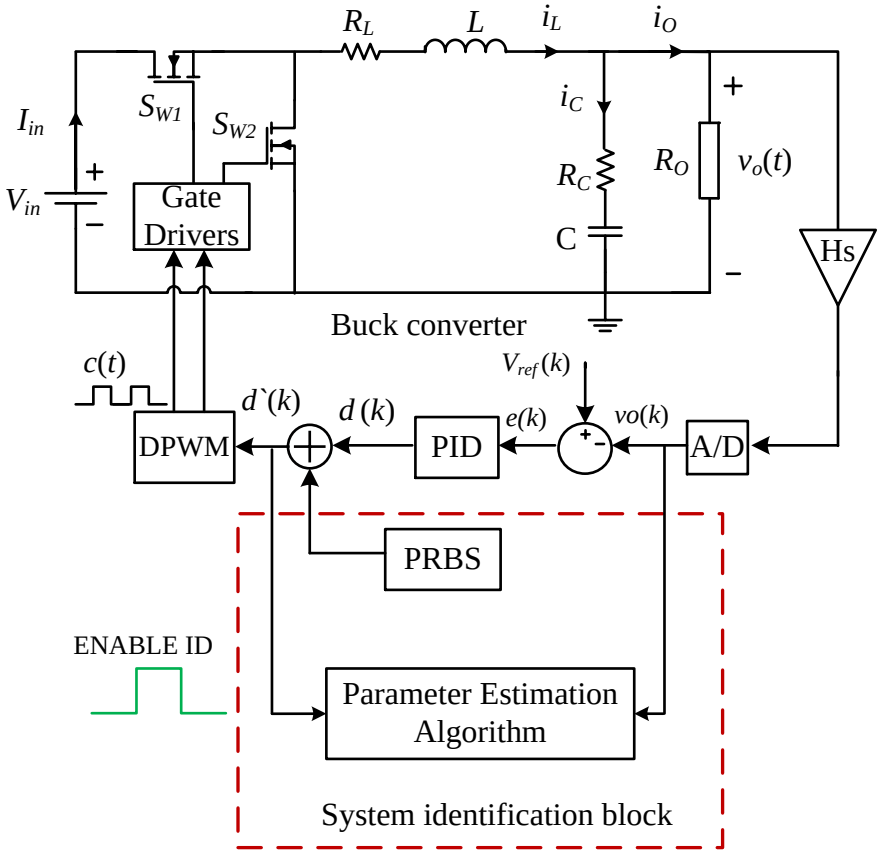


Figure 4.4 The Proposed parametric identification scheme using KF approach

As illustrated in figure 4.4, the control signal $d\,(k)$ is superimposed on a frequency-rich signal or called a perturbation signal to enhance the estimator capabilities in identifying the dynamic behaviour of the system and to improve the overall performance of the identification in terms of accuracy and convergence time. This small excitation signal is injected only during the identification process, and then the converter reverts back to its normal operation. The importance of using an excitation signal is to ensure that the input is persistently excited by means of having a non-singular correlation matrix [6, 68]. This yields more accurate estimation of the discrete model, as the estimated parameters converge to their actual values [6].

4.6.1 *Pseudo-Random Binary Sequence (PRBS)*

In this work, the amplitude-modulated Pseudo-Random-Binary-Sequence (PRBS) signal is selected as a perturbation signal. The PRBS is a periodic and deterministic signal which

can be easily generated using a shift register and an exclusive-or gate (XOR) in the feedback as shown in figure 4.5a. The data length for one period of an *n*-bit maximum length PRBS is given by $M = 2^n - 1$ [4, 75]. This special class of PRBS is called the maximum-length binary sequence (MLBS) [81]. To generate the MLBS, the XOR operation is performed iteratively between the *i*-th register and a particular *j*-th cell register (Table 4.9) [4, 67].

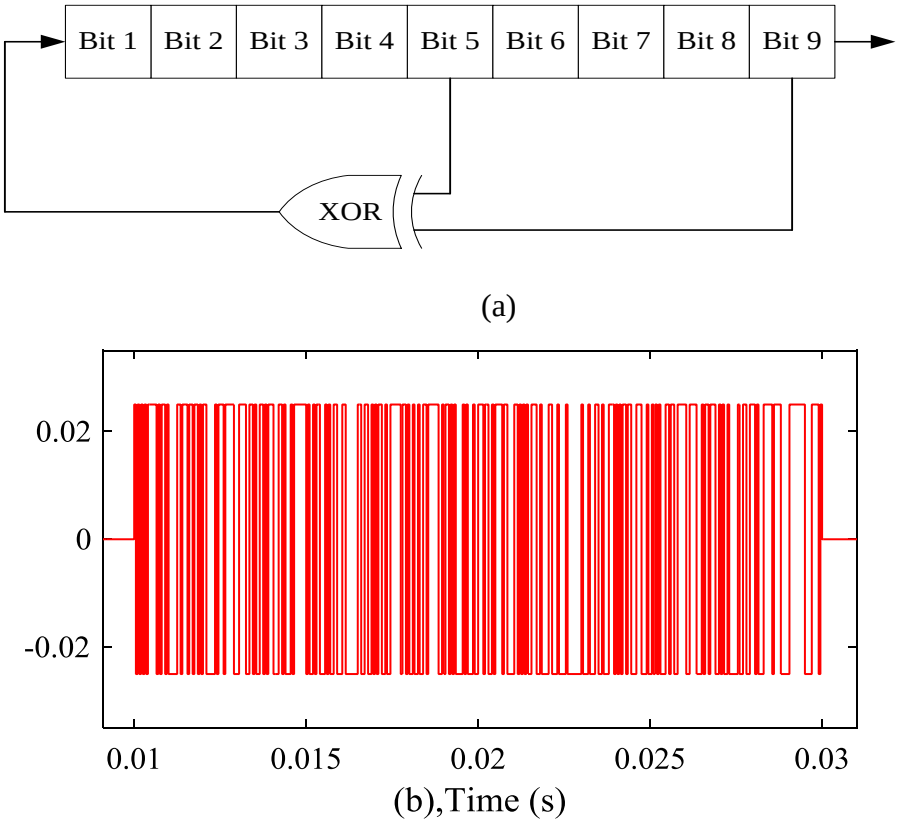


Figure 4.5 Nine-bits shift register with XOR feedback for 511 maximum length PRBS generation

The amplitude of the generated signal has only two possible values; either one representing a positive signal or zero denoting a negative amplitude. The aforementioned steps are applied to generate a 9-bit PRBS signal as shown in Figure 4.5b. Here, the XOR operation is performed between the first and the fifth bits, producing a sequence of maximum length sequence M = 511 before the is repeated [4]. Once this signal is added to the controller output, $d_{copm}(k)$, a perturbed control action is created $d`(k)$, which causes a small disturbance in the duty cycle $c(t)$.

Table 4.5 Bit cell setup for different MLBS generation

Number of bits (n)	$M = 2^n - 1$	Bits in XOR operation *i-th, j-th bits*
2	3	1 and 2
3	7	1 and 3
4	15	3 and 4
5	31	3 and 5
6	63	5 and 6
7	127	4 and 7
8	255	2,3,4, and 8
9	511	5 and 9

4.6.2 *Model Structure Selection*

Another essential step which has to be taken prior to a parametric identification procedure is the selection of the appropriate discrete time modelling of an SMPC. In the proposed scheme, the ARX model is selected as the simplest model structure to approximate the actual behaviour of the studied DC-DC buck converter. This regression ARX model (4.25) is adopted in most adaptive controller designs, due to its simple structure with only a few parameters which need to be estimated using measured input/output data [45, 91]:

$$A(z)y(k) = B(z)u(k) + \varepsilon(k) \tag{4.25}$$

where the term $\varepsilon(k)$ represents the residual error due to noise and parameter uncertainty. Referring to the mathematical model of DC-DC buck converter derived in Chapter 2, the discrete time model can be obtained by means of applying the state space average model to extract the continuous control-to-output transfer function (4.26) as a first step.:

$$G_{dv}(s) = \frac{v_o(s)}{d(s)} = \frac{V_{in}\,(CR_C s + 1)}{s^2 L\,C\left(\frac{R_C + R_o}{R_L + R_o}\right) + S\left(CR_C + C\left(\frac{R_O R_L}{R_O + R_L}\right) + \frac{L}{R_O + R_L}\right) + 1} \tag{4.26}$$

Here the DC-DC buck converter is an SISO physical system, and the input is the control signal $d(s)$ and the output is the measured output voltage $v_o(s)$. According to the literature, for the sake of simplicity and ease of use, the voltage transfer function representation is preferred for control design and health monitoring purposes in DC-DC converters [1, 8, 91]. Given the continuous transfer function in (4.27), the discrete-time model is determined using a

conventional continuous to discrete transformation method such as (ZOH), which results in a second order discrete transfer function as expressed in (4.27).

$$G_{dv}(z)=\frac{b_1 z^{-1}+b_2 z^{-2}}{1+a_1 z^{-1}+a_2 z^{-2}} \tag{4.27}$$

where a_1, a_2, b_1, and b_2 are the parameters to be estimated on-line and their values depend on the physical component values (R, L, C, R_C, R_L) and on the digital sampling time T, which is usually selected to be equal to the converter switching time [8, 83]. The discrete transfer function expressed in (4.27) is described as a linear difference equation suitable for hardware implementation as follows:

$$v_o(k)+a_1 v_o(k-1)+a_2 v_o(k-2)=b_1 d(k-1)+b_2 d(k-2) \tag{4.28}$$

In order to identify the coefficients a_1, a_2, b_1, and b_2, an error is added to the model expressed in (4.28), which takes into account measurement noise and modelling approximations [92]:

$$v_o(k)+\hat{a}_1 v_o(k-1)+\hat{a}_2 v_o(k-2)=\hat{b}_1 d(k-1)+\hat{b}_2 d(k-2)+\varepsilon(k) \tag{4.29}$$

Describing the ARX model structure as initially expressed as in (4.25), one can realise an obvious resemblance between the difference equation (4.29) and a second-order ARX model with b_0 set to zero [92].

4.7 Simulation Results for Steady-State Operation

In order to verify the performance of the proposed identification algorithm, a voltage-controlled synchronous DC–DC buck SMPC circuit was implemented in MATLAB/Simulink (see appendix B). The component values for the converter depicted in figure (4.4) were: V_{in} =10 V, R_O = 5 Ω, L= 220 μH, C=330 μF, R_C =25 mΩ, R_L = 63 mΩ, $R_{DS(on)}$= 18 mΩ, the switching frequency and sampling rate are 20 kHz, and the sensing gain H_s= 0.5. In figure 4.4, the parasitic elements are included to improve model accuracy and to demonstrate the importance of considering non-ideal components for system identification in applications such as power electronics converters. For instance, in the buck converter, the equivalent series resistor R_C cannot be ignored because it adds a zero to the transfer function, which has a negative impact on the dynamic behaviour of the converter [118]. In addition, its value may be used as a diagnostic indicator of capacitor ageing [1].

To justify the identification results, the discrete transfer function of the average model in (4.27) is calculated in advance, at a sampling time of 50 μs. In line with many other studies, convergence time and accuracy are considered to be the important metrics in evaluating the adaptive algorithm's performance [8, 83].

$$G_{dv}(z) = \frac{0.2262\, z^{-1} + 0.1119\, z^{-2}}{1 - 1.913\, z^{-1} + 0.946\, z^{-2}} \tag{4.30}$$

Using the discrete transfer function obtained, a digital PID controller (4.31) is designed based on the pole placement technique to regulate the output voltage at 3.3 V:

$$G_c(z) = \frac{d(z)}{e(z)} = \frac{q_0 + q_1 z^{-1} + q_2 z^{-2}}{(1 - z^{-1})(1 + \gamma z^{-1})} \tag{4.31}$$

In (4.32), q_0= 4.672, $q_1 = -7.539$, q_2 =3.184, and $\gamma = -0.374$. The designed digital controller is simulated and its performance was investigated in Chapter 2. This confirms that, if the discrete transfer function is accurately known, an efficient controller can be designed and the actual circuit component values are determined for condition monitoring use [65]. In practical, the coefficients $[a_1, a_2, b_1, b_2]$ are not constant and can vary over time due to different circumstances, such as component ageing, temperature, and load change. Thus, a parametric system identification process is essential to alleviate any degradation in the overall performance of DC-DC converter and the powered application.

In this work, the conventional ERLS scheme is applied as a test-bed for assessing the performance of the proposed KF algorithm. In the early stages of the estimation process, no preliminary knowledge of the converter parameters is assumed. The same initial values of covariance matrix and parameter vector for both ERLS and KF are selected to be $P(0) = 10000$ I, and $\hat{\theta}(0) = 0$. For the ERLS, the forgetting factor $\lambda = 0.95$ is carefully chosen as a compromise between estimator sensitivity and convergence speed. The modified tuning method in (4.24) is applied to mitigate the disadvantages of using a trial and error procedure in the KF tuning and the measurement noise variance *r* is set to 0.095.

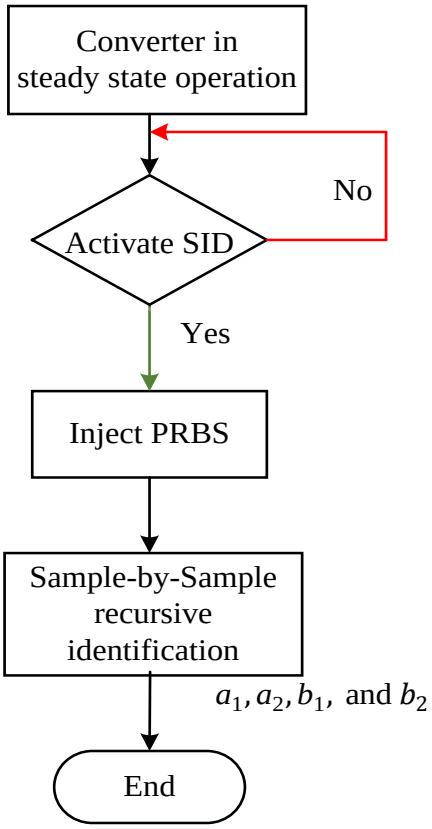


Figure 4.6 The procedure of system identification

In addition to the step-down converter, the Simulink model is constructed identically to that in figure 4.4, and the system identification sequence is performed step by step as described by the flowchart in figure 4.6. Here, the identification procedure is enabled whilst the converter is in steady-state operation as depicted in figure 4.7(a), (b). Simultaneously, a 9-bit PRBS is injected into the feedback loop as a frequency rich excitation signal for 20 ms as shown in figure 4.7(c). This is adequate to demonstrate the convergence time for both adaptive algorithms. In order to avoid causing large ripples in the output voltage, the magnitude of PRBS signal is selected to be ΔPRBS = ± 0.025. This perturbation signal is approximately ± 2.5% with respect to the nominal DC output voltage under normal operating conditions, as shown in figure 4.7(a).

As a pre-processing step, each input/output sample is subtracted from its mean value to remove the offsets to yield a raw data with a zero mean value. Then, the obtained zero mean values of both the sampled power converter output voltage $v_o(k)$, and the control signal $d`(k)$ are used by the identification algorithm (ELRS, KF) to compute and update the adaptive IIR filter coefficients for every sampling instant.

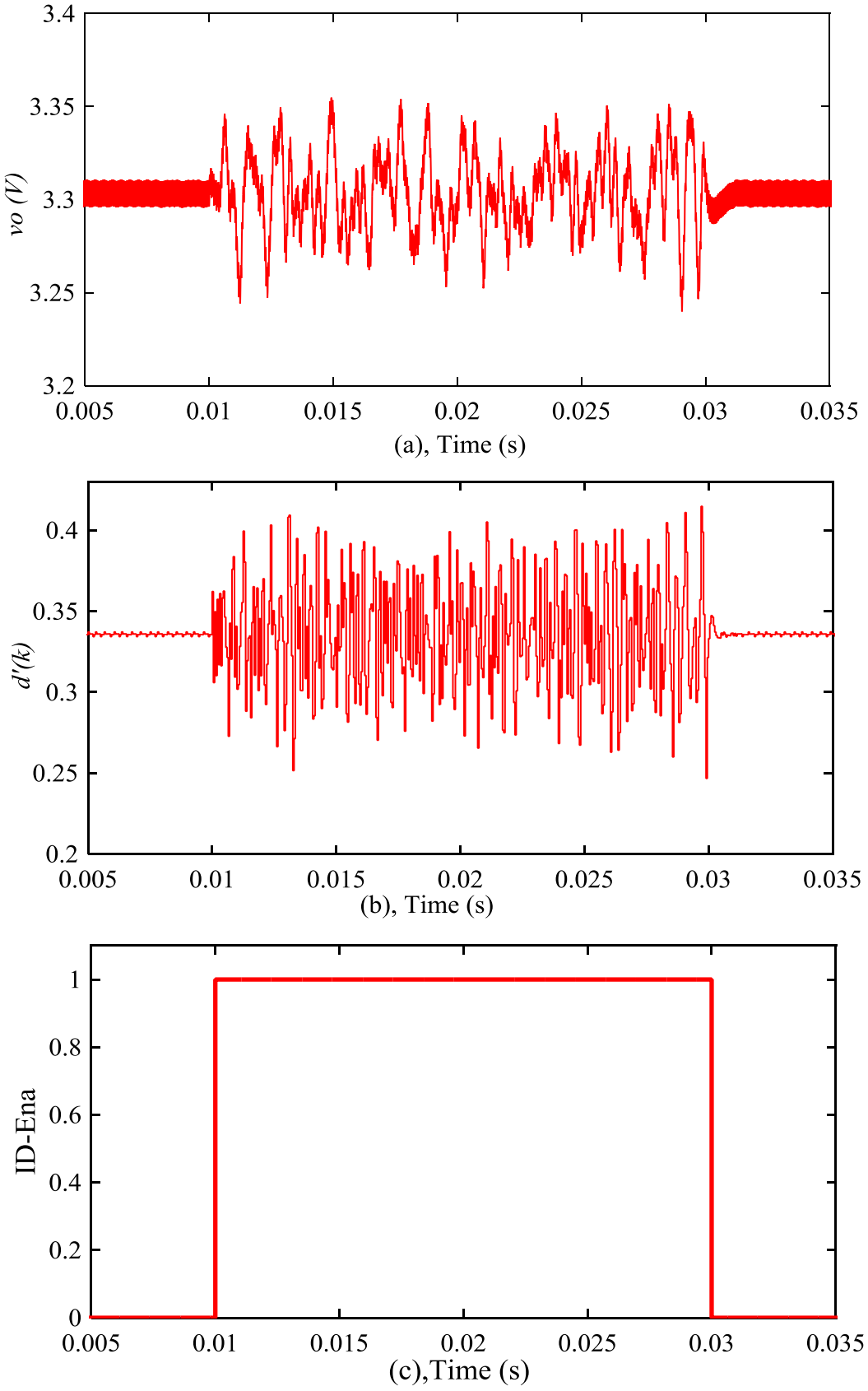


Figure 4.7 Identification sequence: a. output voltage during ID; b. control signal during ID; c. ID enable signal

Figure 4.8 shows the on-line parameter estimation results obtained using the ERLS identification algorithm and KF identification algorithm during the steady state operation. As depicted in figure 4.8, both estimation algorithms rapidly identify the transfer function coefficients with final estimation values very close to the average model in (4.44). However, the KF estimation converges to the steady state in less than 1.5 ms, while the ERLS estimator takes more than 2 ms to reach the final values. To demonstrate the overall performance of the KF scheme, the prediction error between the measured output voltage and the adaptive filter output is illustrated in 4.8(c). Here, the KF estimator minimises the prediction error faster than the classical ERLS algorithm with a smaller overshoot during estimation start-up.

The individual estimation error for each parameter is shown in figure 4.9, where it can be seen that the KF algorithm outperforms the classical ERLS. Figure 4.9(a) demonstrates the comparable convergence for all transfer function coefficients when the KF algorithm is applied. This confirms the effectiveness of the covariance update strategy and the proposed tuning method used in the KF, where each parameter is assigned with a different gain based on its contribution to the overall filter output. In contrast, the convergence time of the ERLS varies between the estimated parameters, due to the effect of the forgetting factor strategy in forming the adaptation gain used in the correction step. The adaptation gains for the largest and the smallest coefficient in the discrete transfer function are illustrated in figure 4.10.

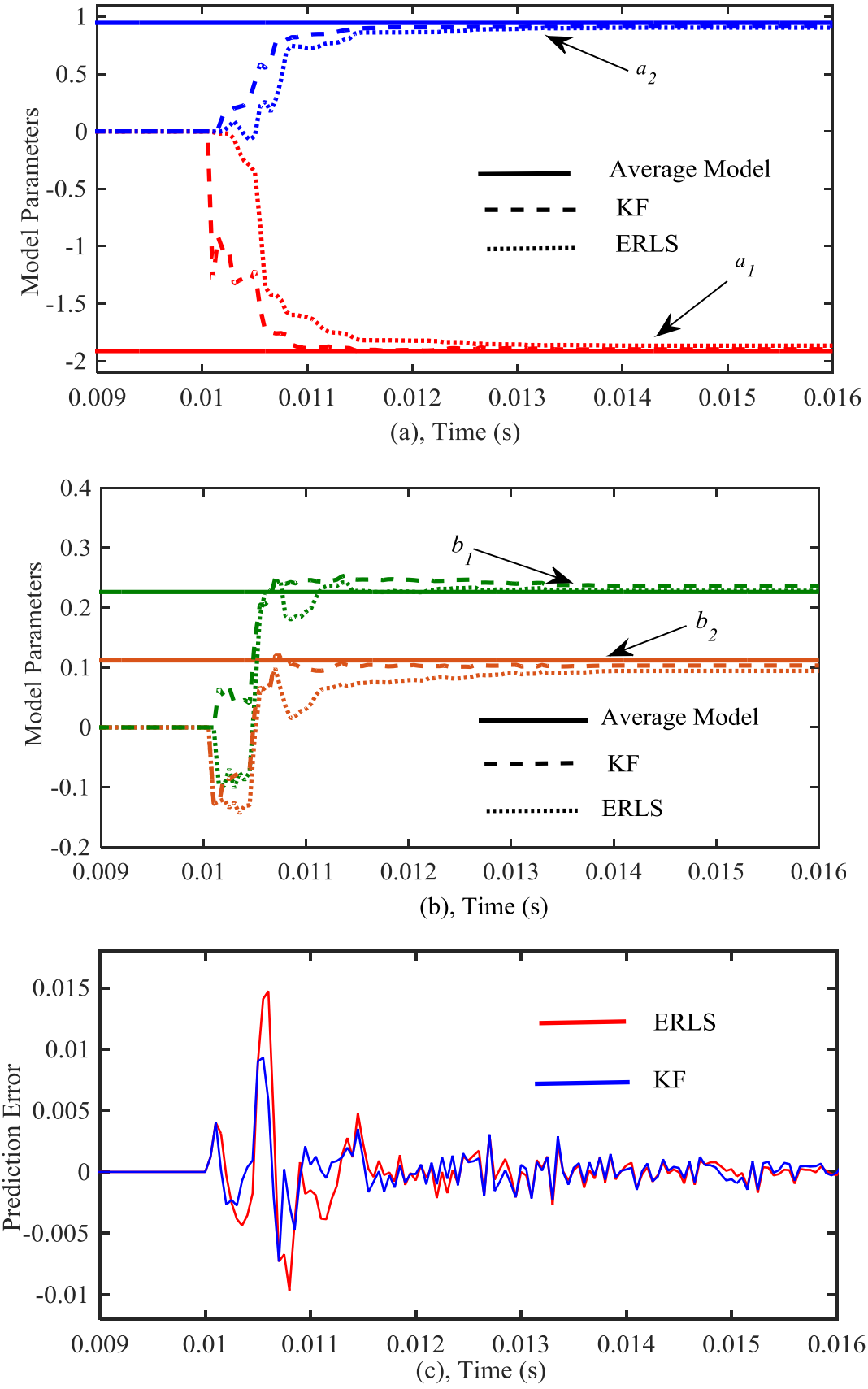


Figure 4.8 On-line parameter estimation results using ERLS and KF: a. denominator coefficients; b. numerator coefficients; c. prediction error

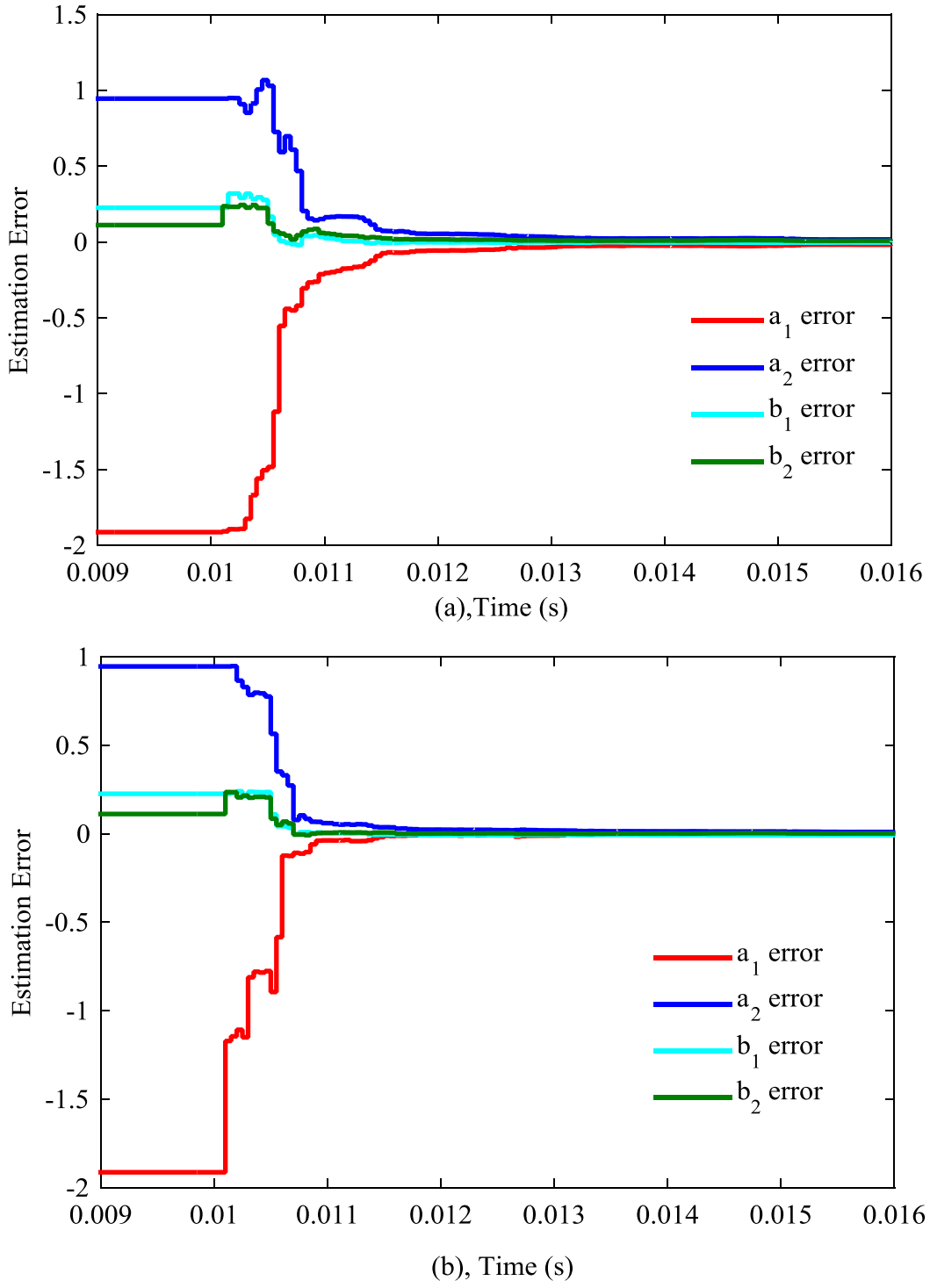


Figure 4.9 Parameters estimation error; a. classical ERLS; b. KF

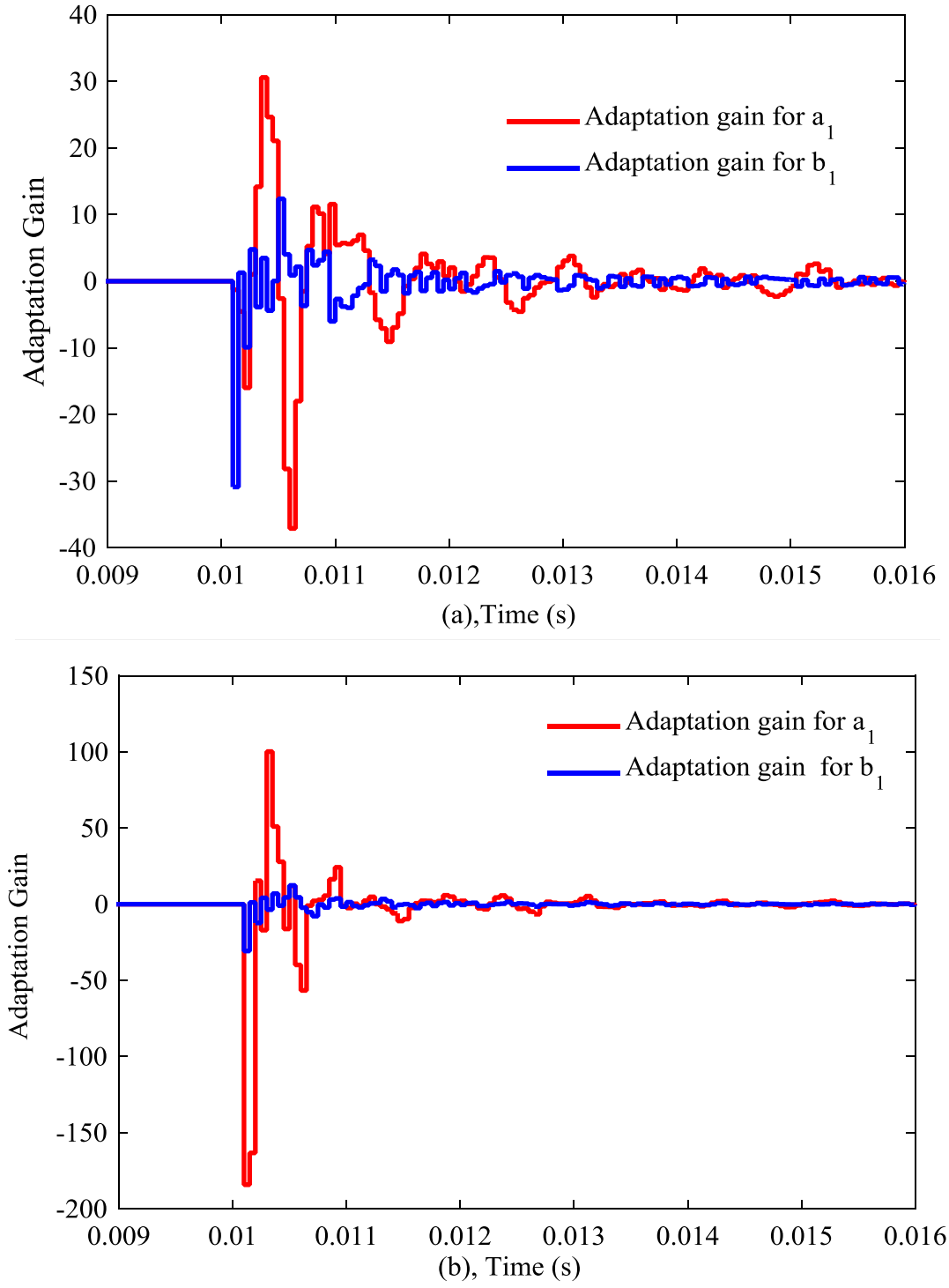


Figure 4.10 Adaptation gain for a_1 and b_1: a. ERLS; b. KF

4.9 Estimator Robustness Against Abrupt Load Change and the Absence of Excitation Signal

It is known that, in SMPC, the mode of operation may be diverted from continuous conducting mode (CCM) to discontinuous conducting (DCM) if a wide load variation is applied, and as a result the loop stability margins are decreased and the converter may exhibit instability during the mode transition [119]. Traditionally, this phenomenon is treated by designing a conservative controller, also known as worst-case design to cope with any abrupt changes and ensure system stability. Therefore, it would be of great benefit if the load value could be estimated and the controller tuned to meet the desired bandwidth and stability margins. For this reason, a wide and abrupt load change is applied to further investigate the performance of the proposed self-tuned KF and compare its performance with the classical ERLS algorithm. Figure 4.11 shows the dynamic response of the output voltage when the load is changing from 5 Ω-to-1 Ω at 0.015 s. In order to justify the identification results, the voltage transfer function model in both load values was calculated in advance as follows:

$$G_{dv}(z) \text{ at } (R_O=5\Omega) = \frac{0.2262 + 0.1119\, z^{-2}}{1\text{-}1.913\, z^{-1} + 0.946\, z^{-2}} \tag{4.32}$$

$$G_{dv}(z) \text{ at } (R_O=1\Omega) = \frac{0.2243\, z^{-1} + 0.1062\, z^{-2}}{1\text{-}1.814\, z^{-1} + 0.8437\, z^{-2}} \tag{4.33}$$

The same identification procedure as outlined in section 4.7 is followed here, with unchanged settings for the PID compensator, PRBS generator, and adaptive algorithms. The denominator parameters [a_1, a_2] are the only parameters in the control-to-output transfer function shown in the estimation results. This is because the load change caused a significant variation in the pole parameters as expressed in equations (4.32) and (4.33), thus making the system disturbance easy to detect. The simulation results presented in figure (4.11) indicate that after a sudden change in the load the KF identifies the transfer function denominator coefficients accurately with a convergence time of less than 1 ms. In contrast, the ERLS estimation exhibited under-or-over shoot before it settled to the final values with a convergence time more than 5 ms.

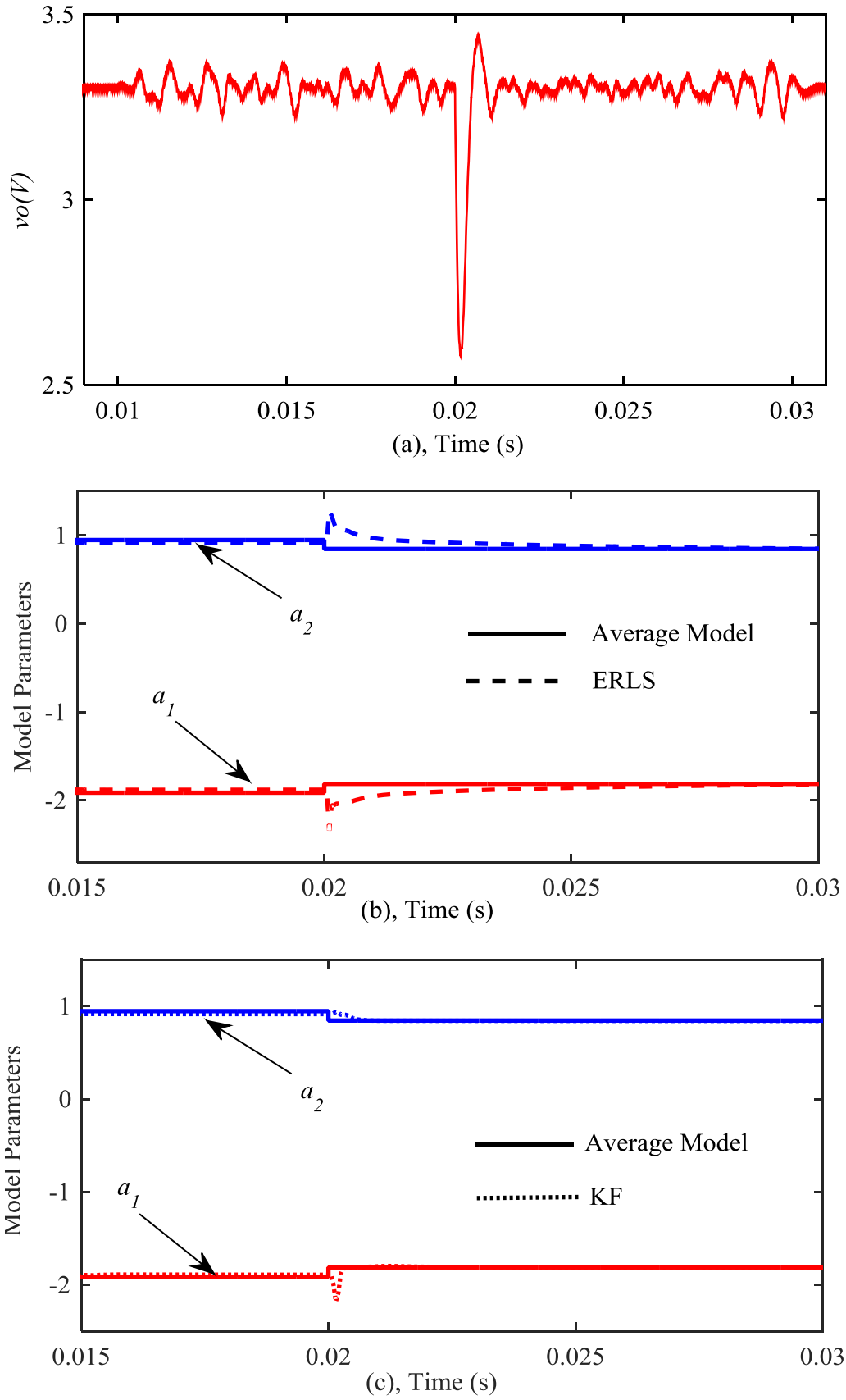
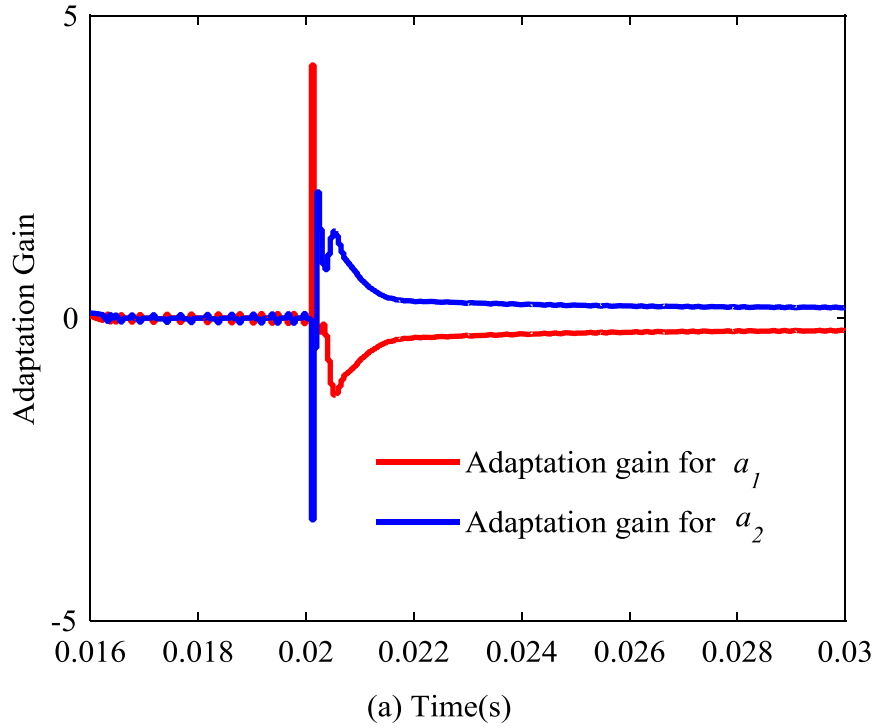


Figure 4.11 On-line parameters estimation during a step load change from 5 Ω to 1 Ω at 0.02 s: a. output voltage; b. ERLS estimation; c. KF estimation

To demonstrate the advantages of using the proposed tuning method for the KF, the related adaptation gains of a_1 and a_2 are recorded in steady state and during the load change as illustrated in figure 4.12(a). As stated in (4.24), each element in the matrix S is tuned according to the contribution of the related parameter vector component in the estimator output $(\varphi_k \hat{\theta}_k)$. Therefore, the assigned Kalman gain elements for K_1 for a1 and K_2 for a_2 vary with different rates in the correction step, yielding good tracking performance of the new applied load. This variation is confirmed by referring to (4.32) and (4.33), where the parameter a_1 decreases by 5.5% of its original value, and at the same time a_2 at 1 Ω reduces by 1% of its value at 5 Ω. This means that the impact of load change varies between one coefficient and another in the discrete transfer function. To compare this with ERLS, the same adaptation gain elements are shown in figure 4.12(b), where it can be seen that similar magnitudes with different directions are applied to both a_1 and a_2 due to the single forgetting factor scheme. Thus, the KF approach is considered to be the ideal candidate in this case to provide reliable estimations of time-varying parameters, such as the load change which is a common scenario in power converter applications.

However, in order to continuously monitor and estimate time-varying parameters such as load changes in DC-DC converters, a perturbation signal is required to be injected into the feedback loop. In some sensitive applications, this kind of continuous perturbation is not desirable. Therefore, there is a need to have an estimator that can work for a longer time with only a very short perturbation period. This scenario is investigated here by means of increasing the identification period to 80 ms and injecting the PRBS signal for 5ms only, as shown in figure 4.13. The estimation results shown in figure 4.13 demonstrate that the KF estimator has the ability to produce a smooth and stable estimation with no effect of estimator wind-up. This is due to the linear growth of the covariance matrix P. Consequently, the KF estimator can work for longer periods without any significant output perturbation and yet continues to exhibit operational responsiveness. In contrast, the ERLS suffers from the estimator wind-up phenomenon as the adaptation gain value increases over time to yield a clear offset in the final estimation value.



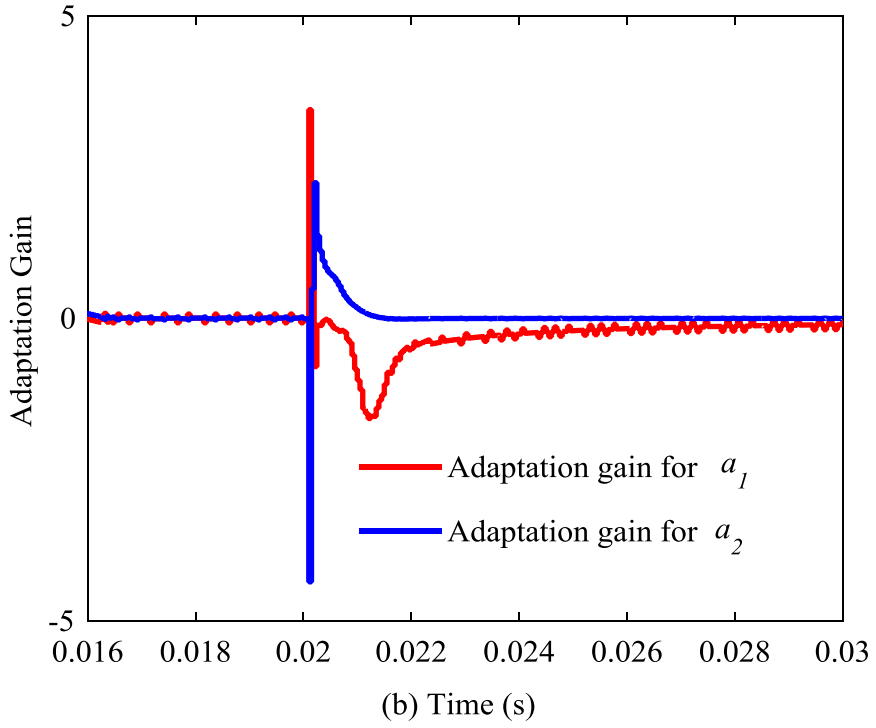


Figure 4.12, Adaptation gain behaviour during abrupt load change: a. ERLS; b. KF

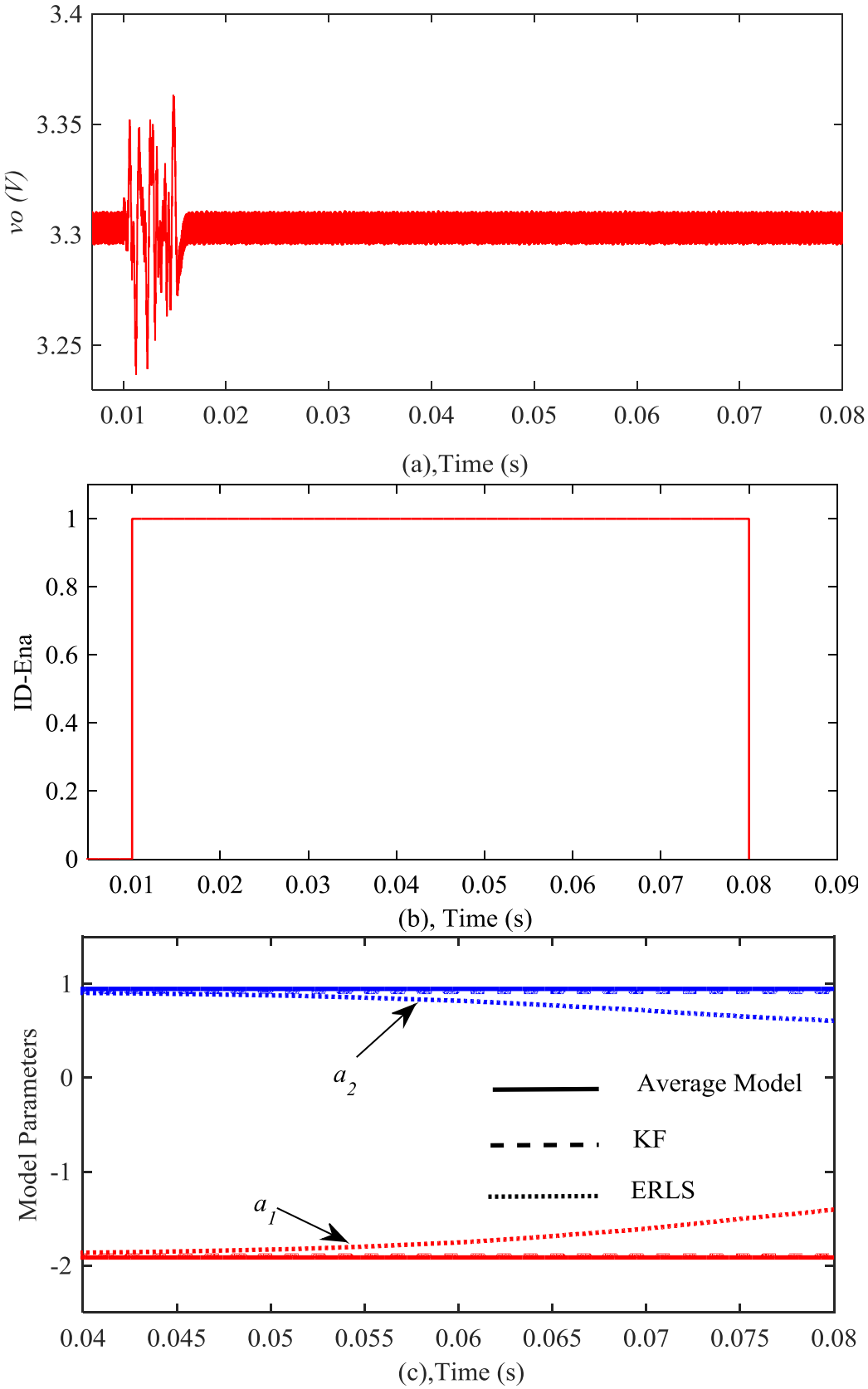


Figure 4.13, Estimator wind-up effect: a. PRBS injected for 5 ms; b.ID enabled for 80 ms; c. voltage model parameters ID

4.10 Chapter Summary

In this chapter further attention is given to adaptive algorithms used in the area of parametric system identification; starting with an overview of the basic LS approach and highlighting the complexity and unsuitability of the LS algorithm for real-time implementations. Recursive parameter estimation is explored, considering the mathematical derivation of the conventional RLS and its extension, the ERLS, to deal with time-varying parameters. The disadvantages of ERLS have been addressed and discussed in detail, particularly in estimating the discrete transfer function of the DC-DC step-down converter. Due to the difficulties experienced with ERLS, the well-known KF state estimator is introduced for parameter estimation purposes to mitigate the shortcomings of ERLS and to enhance overall performance. In addition, a new tuning method for the KF approach is introduced in this chapter to improve the tracking capabilities of the estimator in identifying time-varying parameters. The model structure selection and excitation signal are also discussed in this chapter.

The performance of the KF estimator is validated by simulation and the results show that the convergence rate and the estimation of the model parameter are very good. Simulation results demonstrated that this approach exhibits excellent all round identification metrics (convergence rate, parameters estimation, and prediction error) during steady-state operation. During the identification process, the tracking capability of the KF has been investigated by means of applying an abrupt load change at the output of the DC-DC converter. The simulation results show that the KF reacts very quickly and responds to parameter changes. As a result, the tuning method is successfully employed for the first time in a KF for the purposes of parameter estimation. Finally, the stability of the KF estimator is evaluated with, and without, an excitation signal which demonstrates robust estimation due to the reduced effect of estimator wind-up. This makes the proposed technique very well-suited to real-time power electronics control applications. However, the superior performance obtained using KF approach comes at the cost of a slightly increase in computational burden of the adaptive scheme due to the proposed tuning step. For this reason, the second research contribution of this work is introduced in the next chapter; an improved computationally efficient KF algorithm is developed via adopting a partial update scheme for the first time.

Chapter 5 A Computationally Efficient Self-Tuning Controller for DC-DC Switch Mode Power Converters Based on Partial Update Kalman Filter

5.1 Introduction

It is known that computational complexity is an important factor in evaluating the performance of any adaptive algorithm in real-time applications [8, 120]. For instance, in mobile communications and computing systems, and in particular battery-operated devices, the complexity of any employed algorithm must be kept to a minimum. This is required to reduce power consumption and to extend the battery life, or produce more compact and light-weight physical devices [121]. The algorithms used in these devices are usually those which involve control design for health monitoring purposes [1, 91]. In this work, the KF is introduced for parameter estimation in SMPC and can readily be applied in many battery-operated devices.

The simulation results outlined in chapter 4 show that the KF algorithm can handle the parameter estimation task efficiently with several advantages over the classical ERLS adaptive algorithm. However, this performance comes with increased computational complexity, which is considered as the main concern in terms of implementation [122]. This is clearly demonstrated in Table 4.4, where the computational burden is proportional to the number of parameters to be estimated; in particular, the computation of adaptation gains and the covariance update. These two steps are known to be the bottlenecks of the recursive algorithm, where multiplication of matrices and vectors is required to update the parameter vector at each iteration. In addition, the overall complexity is likely to increase further if the identification algorithm is combined with an adaptive controller or health monitoring scheme in SMPC applications. This necessitates more power consumption, as more hardware multipliers and memory are required [121].

To cope with this increased complexity and to maintain the desired performance, a more powerful and faster microprocessor platform is needed. This implies higher implementation cost, which is particularly undesirable in small, high-volume systems [8]. Therefore, it is

essential to reduce the computational overhead of the adaptive algorithm in order to exploit the system identification results in real-time for adaptive control design and condition monitoring purposes for low-cost hardware. This can be achieved by reducing the computational effort at the software level and hence reducing power consumption [121]. One promising approach to controlling the computational cost of adaptive algorithms is to use a partial update scheme where a subset of the adaptive filter coefficients are updated at each iteration [121, 123-126]. In parametric system identification, the achievable complexity reduction by partial coefficient updates is significant, as a number of key arithmetic operations are eliminated [121]. Several types of partial update methods have been studied in the literature including sequential PU, periodic PU, M-Max PU, stochastic PU, and selective PU [124]. In this work, PU methods are applied to the KF for the first time to reduce the computational overhead while retaining comparable overall performance to the full version.

In addition to the adaptive algorithm, there is a need for a computationally light control strategy to implement an efficient and cost effective self-tuning controller. Therefore, this chapter presents a digital self-tuning Bányász/Keviczky PID controller based on PUKF estimation. In comparison with the previously described pole placement technique, the Bányász/Keviczky PID controller is simple in terms of the number of arithmetic operations required to calculate the controller output. Therefore, the overall complexity of the STC scheme is further reduced, which can be applied in many different applications. .

5.2 Partial Update Adaptive Filter Theory

The partial-update (PU) scheme is a straightforward method to reduce the computational complexity of adaptive filtering algorithms because it only updates part of the parameter vector instead of updating the full filter vector [121, 127]. This means that, instead of updating all of the $N \times 1$ coefficients in the parameter vector, the partial-update method only updates $M \times 1$ coefficients, where $M < N$ [127].

According to the existing literature, PU methods are mostly applied to LMS and its modifications [120, 124, 126, 128-131]. These applied algorithms update a subset of the adaptive filter coefficients at the time of each iteration, either in a sequential or periodic manner, or by using a selection criterion [128]. On the other hand, very few studies have addressed the

use of partial update methods in computationally complex algorithms such as the RLS algorithm [122, 125]. Importantly, all the aforementioned algorithms are applied in the telecommunications field, and most of the results presented so far are from simulation only. Therefore, this work focuses on applying the PU scheme to the KF adaptive algorithm and investigating its performance on-line and in real-time power electronic applications. In addition, the reliability of the proposed approach is further evaluated by means of STC implementation.

5.3 Partial Update Methods

The general concept of a PU scheme can be applied using different methods. Among these methods, data-independent approaches including the periodic PU and the sequential PU [124]. These approaches are the primary ones used to develop PU adaptive algorithms with reduced a computational cost [132]. However, these techniques exhibit slow convergence rates and their overall complexity is proportional to the size of the coefficient subsets in the case of sequential PU and to the update frequency for periodic PU [121, 133].

To enhance the convergence rate, data-dependent PU methods have been proposed and successfully applied to LMS, NLMS, RLS, and AP algorithms [124, 125, 129, 133, 134]. The M-Max and the selective updates are the most commonly used data-dependent PU methods [127, 131]. Here, the update technique is based on finding the subset of the parameter vector that can make the biggest contribution to the filter output and result in the largest reduction in performance error [123]. In other words, for a filter with N coefficients, only the taps corresponding to the M largest magnitude of the data vector are updated at each time iteration [125]. This requires a prior knowledge of the application under consideration. In the parametric system identification of SMPC, this kind of prior knowledge can be acquired from modelling techniques such as SSA and using a model structure such as the ARX model.

As presented in the literature, the M-Max tap-selection criterion provides a level of performance comparable to that of full version adaptive algorithms such as NLMS, RLS, and AP in terms of mean square error and convergence rate [129, 134-136]. The latter metrics are considered to evaluate the performance of the adaptive algorithm in the parametric system identification process. Therefore, this scheme is adopted in this work to perform the PU method in order to maintain the convergence rate and provide accurate estimation of the discrete transfer

function. A detailed description of M-Max PU method is given in the next section, followed by its implementation with the KF algorithm and an analysis of its computational complexity. More detail concerning other PU methods can be found elsewhere [121, 127].

5.4 M-Max Algorithm

The M-Max PU method is a data-dependent partial update technique which was originally proposed by Aboulnasr *et al* [123] with the intention of reducing the computational cost of the NLMS algorithm. Figure 5.1 shows an adaptive filter of length *N* used in a system identification structure, in which the input regression vector is defined as: $x(k) = [x(k), x(k-1), \ldots., x(k-N+1)]^T$, and the filter coefficients vector is given by $\hat{h}(k) = [\hat{h}_1(k), \hat{h}_2(k), \ldots., \hat{h}_N(k)]^T$. During the identification procedure the adaptive filter is used to identify the parameter vector $h(k) = [h_1(k), h_2(k), \ldots., h_N(k)]^T$ by means of minimising the square of the error signal as follows [134]:

$$\varepsilon\,(k) = y(k) - \hat{y}(k) + v(k) \tag{5.1}$$

where $\hat{y}(k) = x^T(k)\hat{h}(k)$ and $v(k)$ is measurement noise. In the M-Max NLMS algorithm, the parameter vector is updated in each time iteration based on a specific selection criterion where only coefficients corresponding to the samples of largest amplitude in the regression vector $x(k)$ are updated [136]. Therefore, the estimation update is computed in a recursive manner given by:

$$\hat{h}(k+1) = \hat{h}(k) + \mu \frac{I_M(k)x(k)\varepsilon\,(k)}{\|x(k)\|^2 + \vartheta} \tag{5.2}$$

where μ and ϑ are the step-size and regularisation parameters respectively, and $I_M(k)$ is the tap selection matrix defined as:

$$I_M(k) = \begin{bmatrix} i_1(k) & 0 & 0 & 0 \\ 0 & i_2(k) & 0 & 0 \\ 0 & 0 & i_3(k) & 0 \\ 0 & 0 & 0 & i_N(k) \end{bmatrix}, i_j(k) = \begin{cases} 1 & |x(k\text{-}j+1)| \in \{\text{M maxima } |x(k)| \\ 0 & \text{otherwise} \end{cases} \tag{5.3}$$

Thus, the M-max updates are simply given by the *M* maxima of the magnitude of the input regression vector entries, which does not require the computation of the full update vector. This

results in complexity reduction for the M-max NLMS algorithm defined by a factor of $B = N/M$ [121].

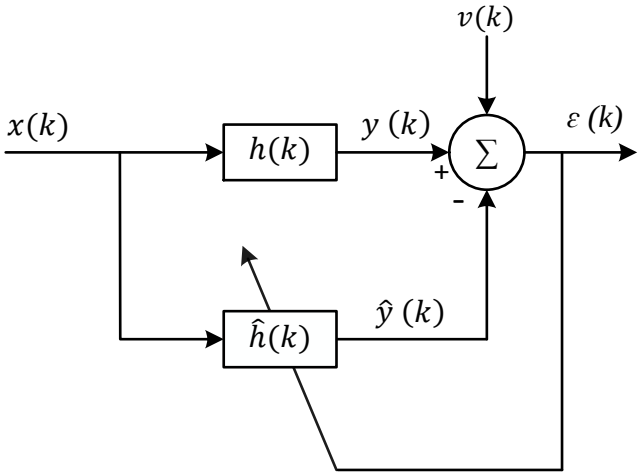


Figure 5.1 System identification structure

5.5 M-Max PUKF

In time-varying systems, the variations of the parameters do not affect the mean prediction error $\varepsilon\ (k)$ equally. Thus, the choice of the filter taps to be updated becomes a vital issue [123]. In this work the KF is introduced to estimate the discrete transfer function of the step-down DC-DC converter. Similarly to the M-Max NLMS, the M-Max algorithm is extended here and applied to the KF algorithm in order to reduce the computational cost of the full version and to produce a new light adaptive algorithm suitable for low-cost implementation. To derive the M-Max KF algorithm, the previously defined ARX model structure is selected to model the buck DC-DC converter and it is expressed in the form of linear regression as follows:

$$v_o(k) = \varphi^T(k)\theta + \varepsilon(k) \tag{5.4}$$

where

$$\varphi(k) = [-v_o(k-1), -v_o(k-2),\ \ d(k-1), d(k-2)]^{\,T} \tag{5.5}$$

$$\theta = [a_1, a_2, b_1, b_2]^T \tag{5.6}$$

According to the basics of the M-Max algorithm, the adaptive filter coefficients corresponding to the largest samples in the regression vector $\varphi(k)$ are selected to be updated. In other words, the update step will consider only the coefficients with the highest error contribution. In the DC-DC buck converter the data vector $\varphi(k)$ consists of the lagged sampled

output voltage $v_o(k)$ and the lagged sampled control signal $d(k)$. In practical applications, the duty cycle is selected to be $0.1 < d(k) < 0.9$, that means when the desired output voltage is higher than 1V, the filter coefficients corresponding to the lagged output voltage are selected to be updated in each time iteration. For instance, in the model example investigated in Chapter 4, the targeted output voltage (v_o) is 3.3 V and the control signal (d) is around 0.33 in steady-state operation. Accordingly, the denominator coefficients $[a_1,a_2]$ are chosen for the update step, as their contribution in the filter output $\hat{v}_1(k)$and hence in the prediction error $\varepsilon(k)$ is higher than the numerator coefficients $[b_1,b_2]$ contribution in the filter output indicated as $\hat{v}_2(k)$. Here, the parameters $[b_1,b_2]$ are considered less important, and the algorithm's performance will only be slightly affected if they are not updated at a given iteration. This results in a 50% complexity reduction compared to the full KF by a factor of $B = N/M$ with N=4 and M=2.

Importantly, in some applications, the accuracy of the estimated parameters is crucial and hence the performance of the PU estimator is required to be as close as possible to the full version. Therefore, the PU algorithm proposed in [122] is adopted here and used to produce a modified version of the original M-Max algorithm. This modification requires the full estimator to be run early in the identification process for a short time, and then the less important parameters are fixed for the rest of the identification period. This means that the only term which will be computed using the full parameter vector with length N is the prediction error at every time iteration. The rest of the algorithm sequence is performed on the sub-filter coefficients with length M. As a result, the prediction error used in the update step describes the contribution of all parameters in the filter output $\hat{v}_o(k)$, and this will produce a more accurate estimation as the less important filter coefficients are considered. In the same manner, the less important coefficients can be updated periodically if needs to be monitored any slow variation, such as ageing in the passive components in the DC-DC converter. Figure 5.2 shows the block diagram of the proposed M-Max PUKF employed in parameter estimation of buck DC-DC converter.

To demonstrate the advantages of the proposed algorithm, Table 5.1 illustrates the required number of arithmetic operations when the proposed M-Max KF is applied and this is compared with the full version of KF in Table 5.2.

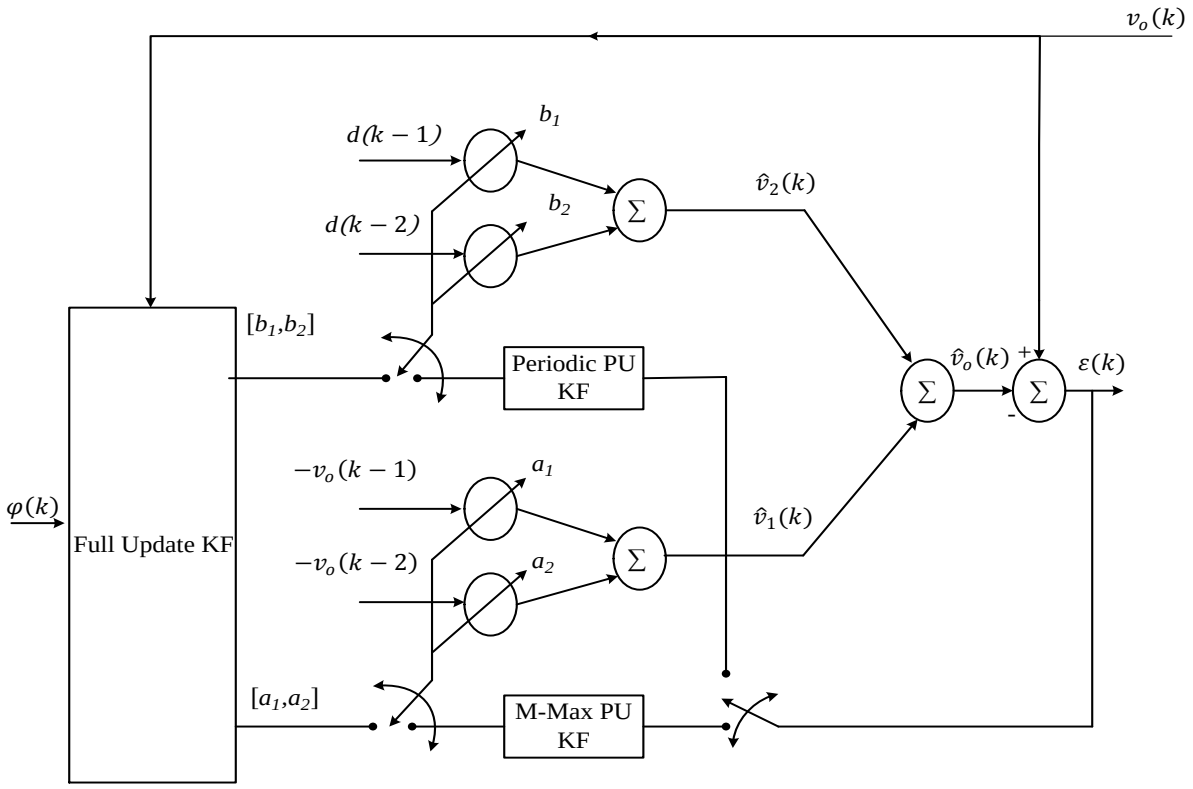


Figure 5.2 The proposed PU scheme.

Table 5.1 Relative computational complexity of the proposed M-Max PUKF

Step	Formula	×	+	÷
Initialisation	$P(0) = g * I$, *and* $\hat{\theta}(0) = 0$, where I is an $M \times M$ identity matrix, g is large number, r is scaler > 0, Q is diag $[Q_{11}, Q_{22}, .., Q_{MM}]$			
	Do for $k \geq 1$			
1	$\varepsilon(k) = y(k) - \varphi^T(k)\hat{\theta}(k-1)$	N	N	-
2	$K(k) = \frac{P(k-1)\varphi(k)}{r + \varphi(k)P(k-1)\varphi^T(k)}$	$2M^2+M$	$2M^2-M$	1
3	$\hat{\theta}(k) = \hat{\theta}(k-1) + K(k)e(k)$	M	M	-
4	$S_{ii}(k) = [K(k)e(k)]^2$	M^2	M	-
5	$P(k+1) = P(k)[I - K(k)\varphi^T(k)] + S$	$2M+M^3$	$2M+M^3$	-

Table 5.2 Relative computational complexity in terms of comparison

Algorithm $N > M$	×	+	÷
Full update KF	$5N+3N^2+N^3$	$4N+2N^2+N^3$	1
M-Max PUKF	$N+4M+3M^2+M^3$	$N+2M^2+3M+M^3$	1

5.6 Digital Self-Tuning Bányász/Keviczky PID Controller

Due to the rapid and significant development in digital signal processors and microcomputers, designing and implementing a complete package of explicit STC has become achievable even for low-cost applications such as SMPC. This package includes an identification algorithm combined with an algebraic control method and/or a health monitoring scheme. This section is devoted to introducing a simple and low-cost discrete PID controller which can be designed on-line in real-time using only the estimation results. This controller was originally developed and introduced by Bányász and Keviczky [137-139], and further investigated for STC design based on the recursive estimation of the process parameters [140]. In practice, the discrete PID regulator is the commonly used strategy in SMPC control scheme. The discrete PID controller can be realised in many different structures based on the selected design approach. As design simplicity is required in this work, the discrete PID controller in its direct form as a two zeros, one pole transfer function is considered:

$$G_C(z) = \frac{q_0 + q_1 z^{-1} + q_2 z^{-2}}{1 - z^{-1}} = \frac{Q(z^{-1})}{1 - z^{-1}} \tag{5.7}$$

For a voltage-mode buck regulator, two zeros are needed to compensate for the second order plant (power stage) and a pole at the origin is needed to minimise steady-state error [29]. In the direct digital control design approach, it is common to construct the regulator based on the inverse of the process model [139]. For that reason, the controlled process is assumed to be a stable, second order dead-time lag with a discrete transfer function given by:

$$G_P(z) = \frac{B(z^{-1})}{A(z^{-1})} = \frac{b_1(1 + \gamma z^{-1})}{1 + a_1 z^{-1} + a_2 z^{-2}} z^{-de} \tag{5.8}$$

where $de > 0$ is the time delay steps of the process, $\gamma = \frac{b_2}{b_1}$, and $b_1 \neq 0$. For the given process specifications, the controller polynomial $Q(z^{-1})$ is chosen to be proportional to the denominator of the controlled process and can be expressed as follows:

$$Q(z^{-1}) = q_0(1 + a_1 z^{-1} + a_2 z^{-2}) = q_0 + q_1 z^{-1} + q_2 z^{-2} \tag{5.9}$$

This implies that:

$$q_1 = q_0 a_1, \qquad q_2 = q_0 a_2 \tag{5.10}$$

The concept of this controller is identical to that of the pole-zero cancellation technique widely used in design using emulation approach [8, 43, 141], where all poles are cancelled and which is applicable for stable processes only. In the practice of tuning this means that the regulator cancels the two largest time constants in the process dynamics. Consequently, the control loop is simplified and given as follows[138]:

$$G_P(z)\ G_C(z) = \frac{k_I(1 + \gamma z^{-1})}{1 - z^{-1}}\ z^{-de} \tag{5.11}$$

Having the reference signal *Ref*(*k*), the closed loop obtained shown in figure 5.3 involves a pure time delay connected in series with an integrator gain that given by the following relationship:

$$k_I = q_0 b_1 \tag{5.12}$$

Having obtained the estimated transfer function coefficients, the controller parameters can finally be computed by the application of the following formulae:

$$q_0 = \frac{k_I}{b_1} \tag{5.13}$$

$$q_1 = q_0 a_1 \tag{5.14}$$

$$q_2 = q_0 a_2 \tag{5.15}$$

$$\text{for } \gamma = 0 \rightarrow k_I = \frac{1}{2de - 1} \tag{5.16}$$

$$\text{for } \gamma > 0 \rightarrow k_I = \frac{1}{2de(1 + \gamma)(1 - \gamma)} \tag{5.17}$$

The relations tips (5.12-5.17) and (5.7) are then used to calculate the controller output as follows:

$$u(k) = q_0 e(k) + q_1 e(k - 1) + q_2 e(k - 2) + u(k - 1) \tag{5.18}$$

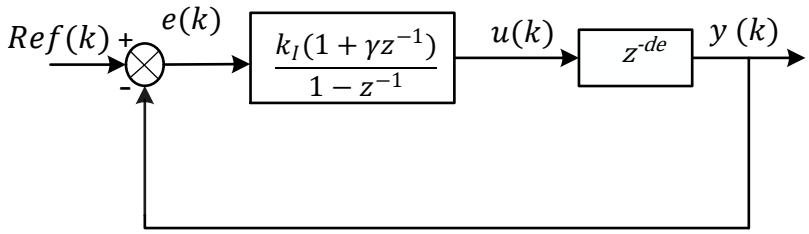


Figure 5.3 Simplified closed-loop system for optimal design.

5.7 Simulation Results

To investigate the overall performance of the proposed explicit STC scheme, a voltage controlled synchronous DC-DC buck SMPC circuit is simulated using MATLAB/Simulink as depicted in figure 5.4. The circuit parameters of the buck converter are as follows: R_o = 5 Ω, R_L = 63 mΩ, R_C = 25 mΩ, L = 220 μH, C = 330 μF, v_o = 3.3 V, and V_{in} = 10 V. The buck converter is switched at 20 kHz using conventional pulse width modulation. The output voltage is also sampled every 50 μs. To demonstrate the parameter estimation task using the proposed M-Max PUKF, the same conditions as in the estimation procedure outlined in Chapter 4 were applied, including PRBS generation and the fixed gains PID controller to initially regulate the output voltage at 3.3 V. In order to imitate the practical case, all of the digital effects were considered in the simulated model, such as ADC, quantisation, and sample and hold delays (see appendix B). For the KF estimator and the M-Max PUKF, the algorithm's initial values are selected to be P (0) = 10000 I, and $\hat{\theta}$ (0) = 0.

As shown in figure 5.4, at the beginning of the identification procedure, a 9-bit PRBS signal is injected into the loop for 25 ms using the 'Enable 1', and during this period the full KF is activated using the 'Enable 2' block for 10 ms, to identify the full parameter vector $[a_1, a_2, b_1, b_2]$ as shown in figure 5.5. After the first stage is accomplished, the numerator coefficients $[b_1, b_2]$ are fixed and exported to the M-Max PUKF and to the ST PID block. Once the full update KF is disabled, the M-Max PUKF is enabled (Enable 3) and the update of the denominator coefficients $[a_1, a_2]$ commences at each time iteration for the rest of the identification procedure.

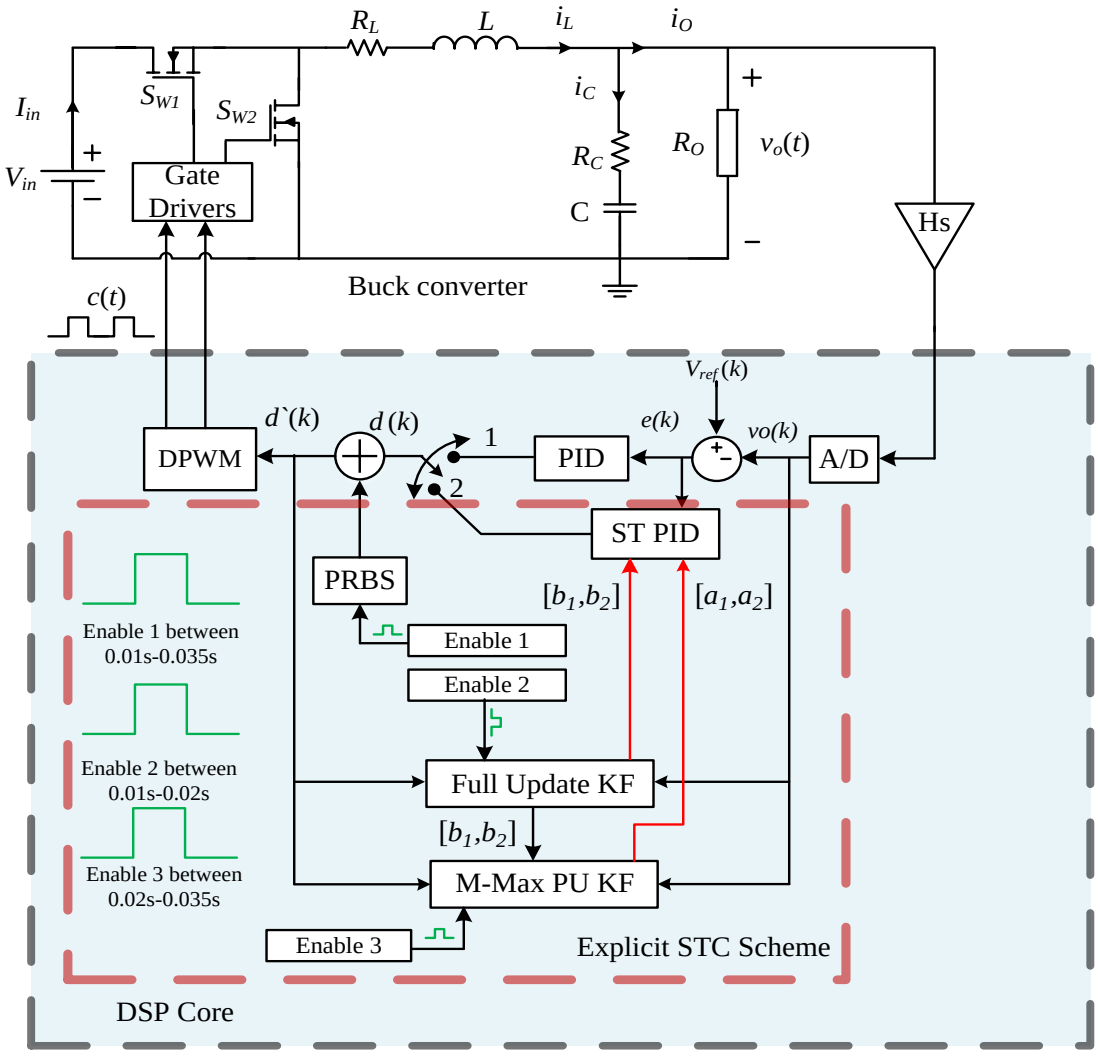


Figure 5.4 Explicit STC using M-Max PUKF

Figure 5.6 illustrates the on-line parameter estimation results obtained using the M-Max PUKF algorithm. Here, the proposed adaptive algorithm rapidly identifies the selected subset of the adaptive filter coefficients $[a_1,a_2]$ with final estimation values very close to the full KF and within the same convergence time of about 1 ms figure 5.6(a). Additionally, the prediction error converges to zero, indicating the good performance of the PUKF (figure 5.6(b)), which is confirmed by the individual estimation error of each coefficient in respect of the calculated average model as depicted in figure 5.6(c).

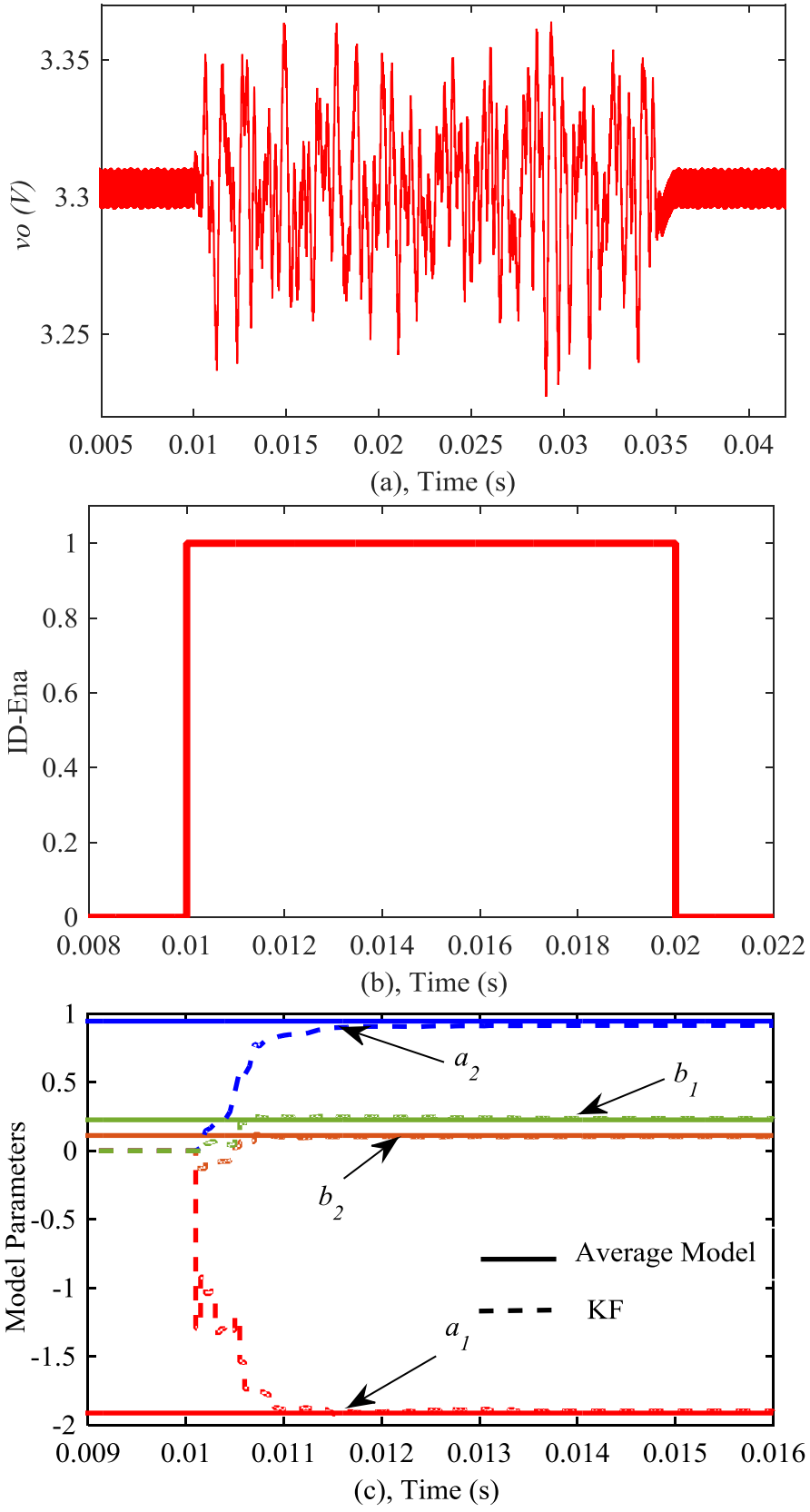


Figure 5.5 Identification sequence: a. output voltage during enable 1 period; b. enable 2 signal for full KF; c. estimated model parameters using full KF

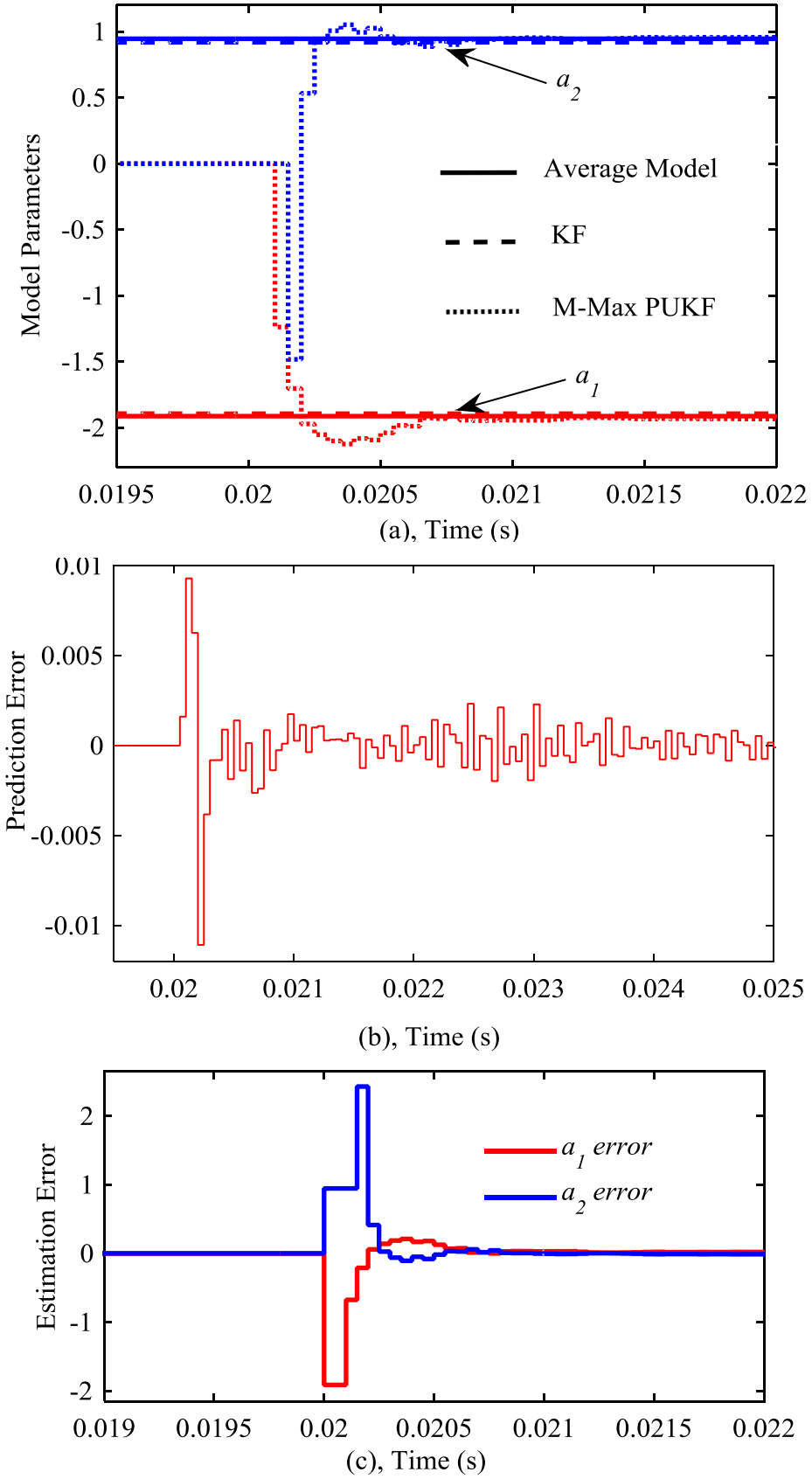


Figure 5.6 On-line parameter estimation results using M-Max PUKF: a. denominator coefficients; b. Prediction error; c. Parameters estimation error

After the PRBS signal is disabled, the discrete transfer function is fully estimated. Now the control action can be computed on-line using the previously described self-tuning Bányász/Keviczky PID controller in the ST PID block, and then the position 2 in the switch is selected to regulate the output voltage by means of explicit the STC designed based on the pole-zero cancellation method using only the estimated discrete transfer function. In SMPC, a significant load variation can occur unexpectedly. Therefore, a derivative action is added to the designed STC to damp out any oscillation caused by the pure integral gain obtained in (5.11), and the controller output is determined as:

$$d(k) = q_0 e(k) + q_1 e(k-1) + q_2 e(k-2) + d(k-1) + K_D[e(k) + e(k-1)] \tag{5.19}$$

The simulation results shown in figure 5.7 demonstrate that the designed STC controller is able to maintain the output voltage at the desired value once it is appointed as the main controller. To study the dynamic behaviour of the proposed STC scheme, a periodic step load change from 5 Ω to 2.5 Ω starting at 0.05 s is introduced. This load change forces the load current to switch between 0.66 A and 1.32 A every 10ms (figure 5.7(b)). As depicted in figure 5.7(a), when an abrupt load change is applied, quick recovery with small overshoot and undershoot to the reference value is accomplished, with the maximum overshoot kept to less than 5% of the desired output voltage. This performance demonstrates the successful design of the proposed STC scheme with the Bányász/Keviczky PID as a control method and the M-Max PUKF algorithm for online parameter estimation.

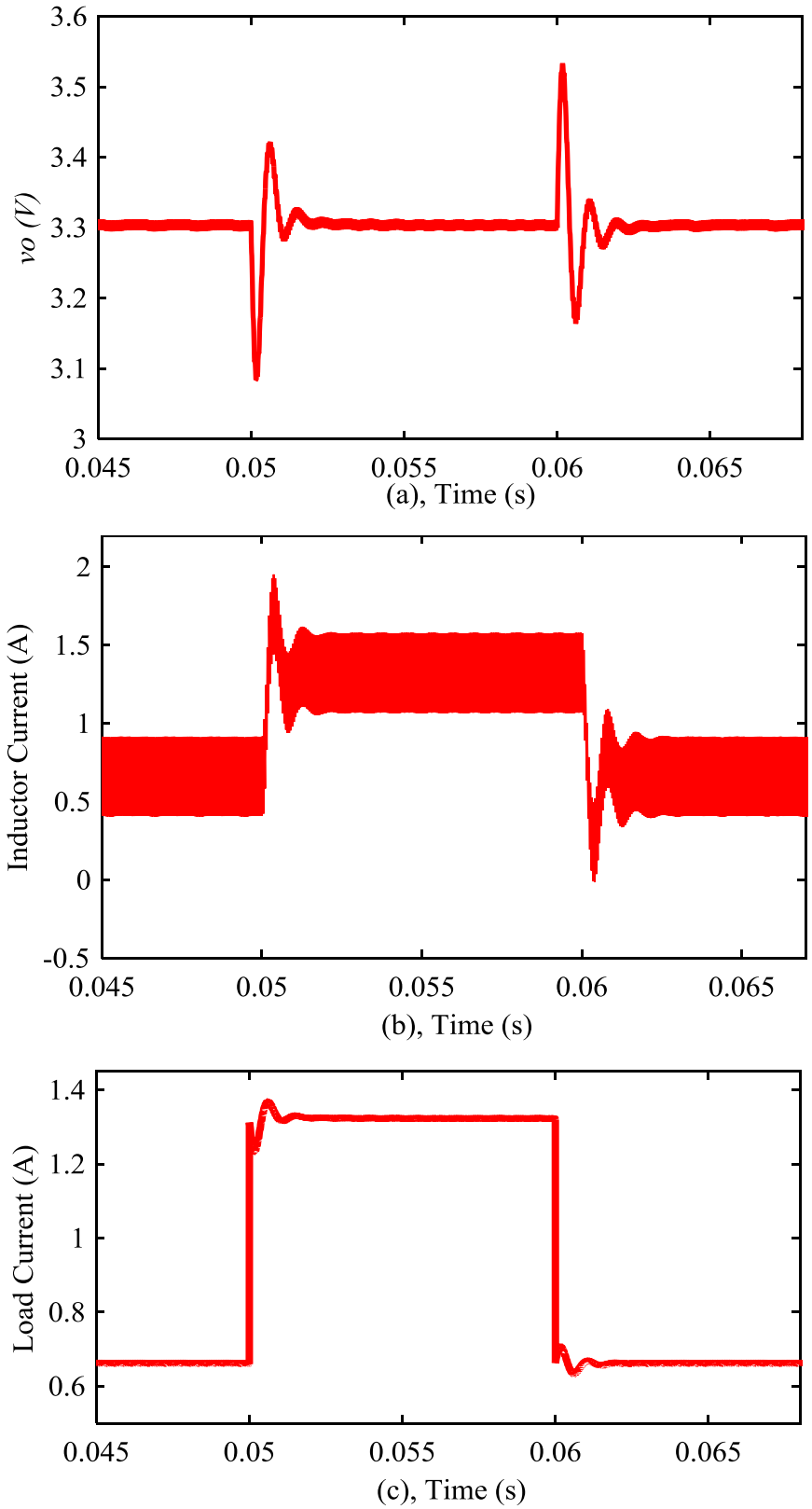


Figure 5.7 Transient response of the proposed STC with *de* =2 and K_D= 0.5: a. output voltage; b. inductor current; c. load current change between 0.66 A and 1.32 A every 10 ms

The same procedure is repeated to evaluate the robustness of the controller and the proposed estimator by means of applying a significant load step from 5 Ω to 1 Ω at 0.05 s. After the load change is detected, a 9-bit PRBS signal is injected to perturb the output voltage for 5 ms in order to update the estimated transfer function as shown in figure 5.9(a). This improves the estimation accuracy and convergence time. At the same time, the M-Max PUKF block is enabled to identify the selected subset of the adaptive filter coefficients $[a_1, a_2]$ in every time iteration. Figure 5.9(b) illustrates the identification results using the M-Max PUKF technique. The transfer function poles are compared to the pre-calculated parameters at 1 Ω and show a very good match. Moreover, it can be seen that the estimation converges to steady-state values in less than 2 ms and the prediction error converges to a small value very close to zero within the same time as shown in figure 5.9(c). Having the new estimated load value, the controller action is updated on-line and the estimator block disabled to reduce the computational load at steady state. This typical scenario is commonly applied in this field, as the estimator block can be activated again if a significant change in the loop error is detected [8, 83, 142].

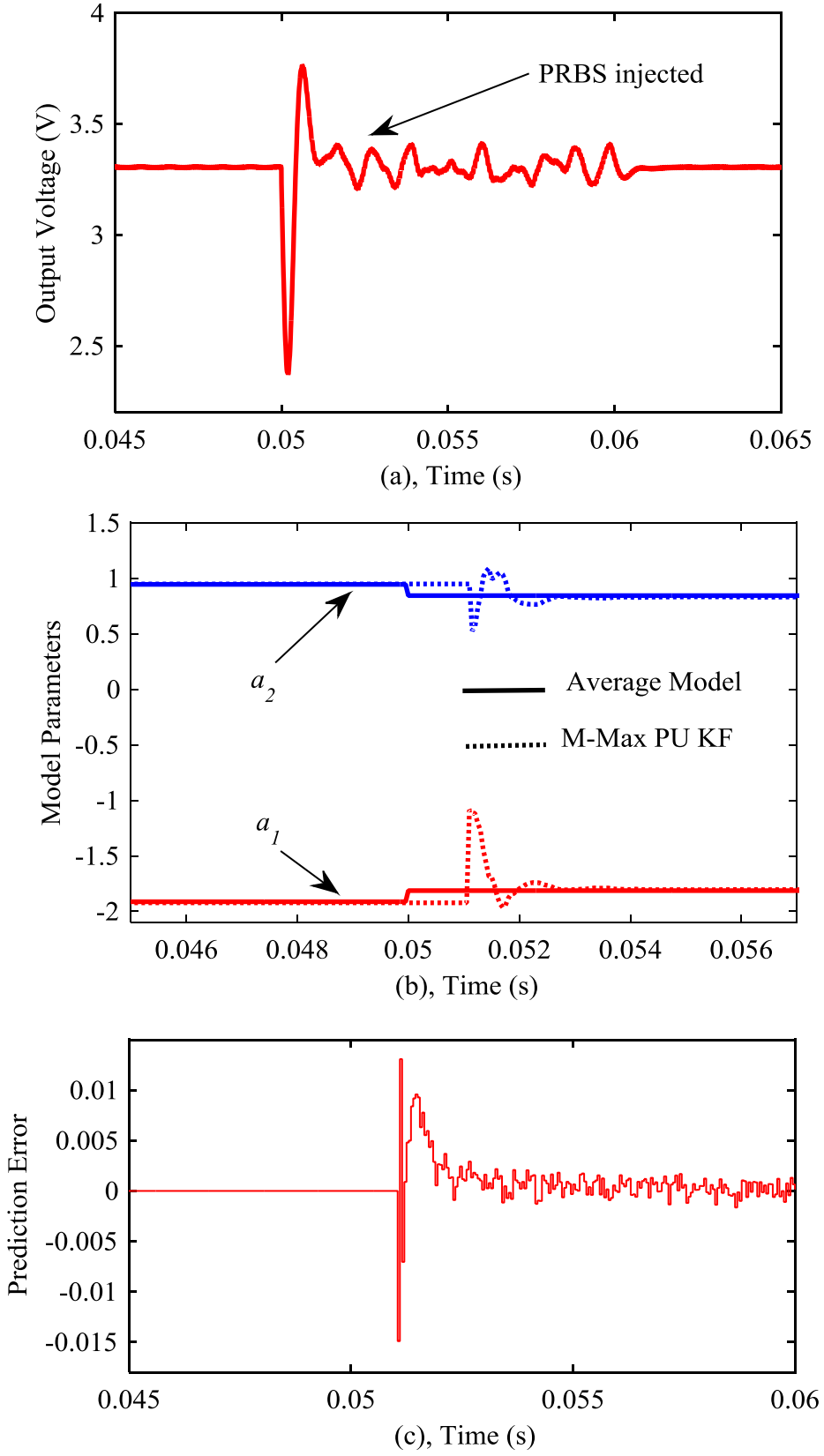


Figure 5.8 On-line parameters estimation during a step load change from 5 Ω to 1 Ω at 0.05 s: a. Output voltage; b. PUKF estimation; c. Prediction error

According to the simulation results, the applied concept of the M-Max PUKF is proven to be a reliable algorithm which can be employed in parametric system identification and in an optimal explicit STC scheme. As the less important coefficients [b_1,b_2] are fixed during the steady state and when the load change is applied, their small effect on the prediction error and on the accuracy of the proposed M-Max PUKF algorithm is clearly observed. The obtained estimation results using the identification scheme in figure 5.4 are compared and presented in Table 5.3 with the average model and full KF estimation at 5 Ω and at 1 Ω.

Table 5.3 Discrete time control-to-output transfer function identification

Parameter		KF	M-MAX PUKF	Model
at 5 Ω	a_1	-1.897	-1.923	-1.913
	a_2	0.9233	0.950	0.945
	b_1	0.2321	fixed 0.2321	0.2259
	b_2	0.1023	fixed 0.1023	0.1118
at 1 Ω	a_1	-1.8	-1.840	-1.814
	a_2	0.822	0.852	0.8437
	b_1	0.219	fixed 0.2321	0.2243
	b_2	0.096	fixed 0.1023	0.1062

As illustrated in Table 5.3, the effect of load change on b_1 and b_2 is very small and can be ignored, which allows the estimator to identify the new values of a_1 and a_2 accurately after a step load change is applied with 0.002 s convergence time and 1.4% estimation error for a_1 and around 1% estimation error for a_2. Moreover, in SMPCs the absolute values of numerator coefficients are further minimised as the switching frequency is increased [8, 143]. Therefore, their corresponding formulae (5.12, 5.13, and 5.17) in computing the controller parameters can be computed only once and used for all load values. This results in an additional 50% complexity reduction in the proposed STC scheme as illustrated in Table 5.4. Here, only the denominator coefficients are updated in each time iteration as they are important in stability analysis and in the pole-zero cancellation technique adopted in the Bányász/Keviczky PID controller.

Table 5.4 Computational complexity reduction in the proposed STC scheme

STC scheme	×	+	÷
Bányász/Keviczky PID and KF	12	6	3
Bányász/Keviczky PID and PUKF	6	3	-

5.8 Chapter Summary

This chapter demonstrates the viability of a low complexity self-tuning control scheme for a DC-DC buck converter. A computationally efficient M-Max PUKF algorithm is introduced to estimate the discrete transfer function partially during the identification procedure. The proposed algorithm achieves around 50% computational complexity reduction in comparison with the full version described in Chapter 4. The concept of this algorithm is based on the data vector analysis in order to select the more important subset of the adaptive filter coefficients to be updated on a cycle-by-cycle basis. Another important aspect covered in this chapter is the adoption of a simple and robust control design method suitable for real time power electronic applications. With a minimum number of arithmetic operations, the self-tuning digital Bányász/Keviczky PID controller has been chosen as the main controller in the proposed STC scheme. In addition, the dynamic performance of the controller and the developed estimator have been investigated in this chapter. The simulation results demonstrate the feasibility of using the PU approach in parameter estimation for DC-DC converters, since the parameter variation are detected and estimated accurately. Furthermore, the controller has been designed on-line using only the estimation results. The proposed controller has the ability to work continuously in the feedback loop and to rapidly recover the output voltage after any load variations. Consequently, the proposed STC scheme is suitable for on-line controller adaptation and has the ability to provide accurate estimation for health monitoring purposes. Finally, the accuracy of the final estimation and the overall complexity reduction have also been explained in this chapter. The following Chapter provides experimental validation of this work.

Chapter 6 Experimental Validation

6.1 Introduction

Even though incorporating digital control in power electronics applications has existed for the last 20 years, only recently has the implementation of advanced signal processing algorithms and intelligent adaptive controllers become feasible. This is achieved due to the continuous fall in prices, and developments in the processing power of microprocessor platforms. However, in the area of system identification, most existing studies run the identification algorithm off-line using real-time data, and then the results obtained are used in control design or condition monitoring schemes for the power electronic application considered. Therefore, a complete real-time implementation is conducted experimentally in this chapter in order to fully corroborate the schemes developed in this thesis. The experimental validation is performed using a 5 W synchronous DC-DC buck converter. The converter is digitally controlled by means of a Texas Instruments TMS320F28335 digital signal processor (DSP) platform. In addition to the digital controller, the DSP hosts the identification process and the STC scheme. The selection of this DSP controller has been motivated by its features such as its embedded floating point unit, and high speed high resolution on-chip ADCs. This chapter describes the real-time implementation and presents research results validating the system identification method using the KF algorithm presented in Chapter 4 and the STC scheme described in Chapter 5.

6.2 Digital Signal Processor

In this research the TMS320F28335-DSP platform is used for on-line parameter estimation and for the STC design of the DC-DC SMPC. This chip is a floating point processor which operates at speeds up to 150 MHz, and it belongs to the TMS320C28x generation from Texas Instruments, optimised for digital control applications. In this generation, the DSP core is integrated with on-chip peripherals to provide a high-performance solution to digital control in power electronics, including motor drive and power supply controllers [144, 145]. The floating point feature allows the TMS320F28335-DSP to perform computationally advanced

algorithms hence simplifying the software design requirements [146]. Figure 6.1 shows the architecture of the TMS320F28335.

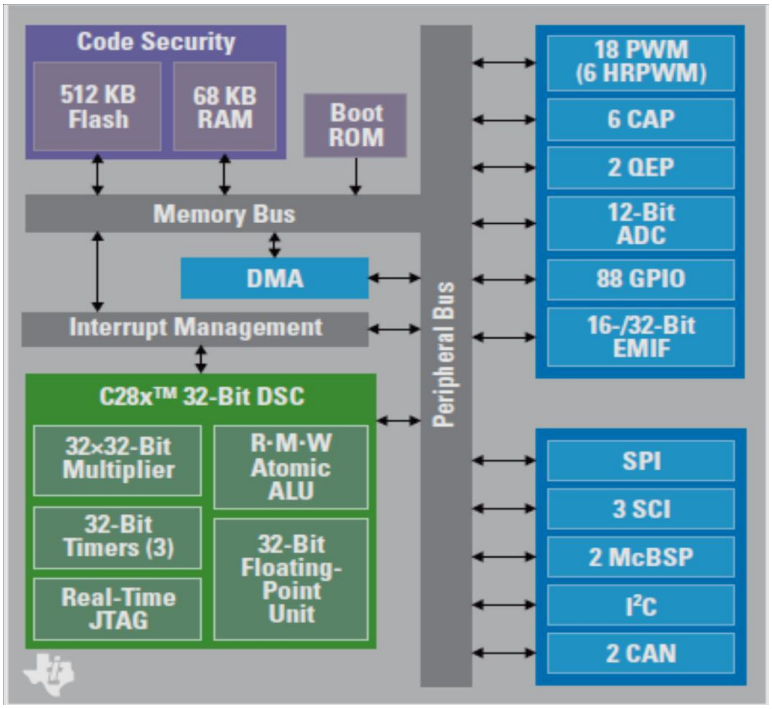


Figure 6.1 Block diagram of TMS320F28335 [146]

As shown in figure 6.1, this platform contains 68 KB data RAM and 512 KB of flash memory for code, so that code can be executed internally without having too costly external memories. The TMS320F28335 supports 32-bit CPU timers, 32-bit floating point units (FPUs), and several serial communication peripherals including the Enhanced Controller Area Network (eCAN), Serial Peripheral Interface (SPI), and Serial Communications Interface (SCI). In addition, many peripherals are integrated on the TMS320F28335 and widely used for embedded control, such as an extremely fast 12-bit ADC that handles up to 16 channels, a memory interface that is configurable for either 16 or 32 bits, and 18 PWM outputs that include six high-resolution PWMs for controlling up to three three-phase motors [146]. In an embedded controller, ADC and PWM modules are the most used peripherals, therefore, more relevant details and explanations of these peripherals in TMS320F28335 are given in the following sections.

6.2.1 *Analog to Digital Converter (ADC) Module*

In digital control applications, it is required to read physical signals such as current and voltage in order to apply the appropriate control action. This task is handled by the ADC unit,

which works as an interface between the controller and the real world. The ADC converts the measured analogue voltage V_{in} into a digital number can be used in the processor for control signal computation. In case of the TMS320F28335, the analogue voltage range is limited to between 0 to 3V. With internal 12-bit resolution, the converted digital voltage (D) is computed in each sampling instant as follows:

$$D = \frac{V_{in} * 4095}{3} \tag{6.1}$$

The ADC of the TMS320F28335 provides a 12-bit core with built-in dual sample-and-hold (S/H), simultaneous sampling or sequential sampling modes, a very fast conversion time (running at 25 MHz), ADC clock or 12.5 MSPS, and 16-channel, multiplexed inputs and 16 result registers to store the converted values. The sequencer of the ADC can be operated as two independent 8-state sequencers or as one large 16-state sequencer. The conversion operation can be started by a trigger signal generated by an event manager or by an external trigger signal through the general purpose input/output (GPIO). Two events (EVA, EVB) are used to trigger the ADCs, and these events can work independently.

6.2.2 *Enhanced Pulse Width Modulation (ePWM) Module*

In many power electronics systems, the control action is applied in the form of a PWM signal. These systems include digital motor control, switch mode power supply control, uninterruptible power supplies (UPS), and other forms of power conversion. The ePWM peripheral executes a digital-to-analogue (DAC) function, where the duty cycle amounts to a DAC analogue value; it is sometimes denoted to as Power DAC [147]. The TMS320F28335-DSP is equipped with dual 6-channel/16-bit enhanced PWM. Each channel can be independently programmed to generate symmetrical and asymmetrical PWM. Each event manager module has a 16-bit general purpose timer. To generate the appropriate duty cycle, the associated control signal is compared with the timer registers using the PWM's compare registers. The timers can be set as up/down counters to imitate the PWM operation. The TMS320F28335 processor also has 6-channels/32-bit enhanced capture input (eCAP) that can be configured to generate 6 PWM channels. The TMS320F28335 provides a programmable dead-band for the PWM output pairs, and the minimum dead-band duration of one device clock cycle (6.67 ns). In DC-DC converters this feature is used to prevent both switches from conducting at the same time [147].

6.3 Code Development Tool

In order to realise and assess the proposed system identification and STC algorithms on the TMS320F28335 DSP the Embedded Coder Support package for C2000 in MATLAB/Simulink is used on the host PC to configure the input/output modules such as the ePWM, ADC, and SCI peripherals and to convert the Simulink model to an executable C code (see appendix C). This in turn allows the designer to utilise the developed Simulink model at the simulation stage, which provides a reasonable comparison between simulation and experimental results. After the executable file is generated, the next step is to download it onto the DSP using the Texas Instruments Code Composer Studio (CCS)-based Integrated Development Environment (IDE).

Finally, the configured Simulink model is run in real time using External mode. In this mode, the Simulink block diagram is connected to the application that runs the model on the DSP via an RS232 communication interface SCI_A. The block diagram becomes a user interface for the real-time application. This feature enables the user to tune and monitor the algorithm's parameters in the real-time application while it is running in real-time without the need to stop the application and modify the code. Moreover, the signals from real-time application can be captured and displayed in the same Simulink Scope blocks which are used for simulating the model [148]. Thus, by adopting this procedure in code development stage, the modelling, algorithm design, simulation and real-time control are fully integrated, which can greatly improve the development efficiency of real-time control systems.

6.4 Experimental Set-up of a Synchronous Buck Converter for Real-time Parameter Estimation and STC

A hardware overview of the entire test platform is shown in figure 6.2, which includes a single-phase synchronous DC-DC buck converter with a dynamic load change circuit, gate drive circuits, signal conditioning/measurement circuits, a separate power supply, and the TMS320F28335 DSP connected to a host PC via a USB serial cable. The synchronous DC-DC buck converter is constructed from a dual N-channel power MOSFET circuit (STS9D8NH3LL) for the upper and lower switches, power stage filter (L and C), a bench power supply for the DC input, and a restive load on the output. To investigate the dynamic performance of the

proposed KF estimator and the designed STC, a dynamic load change circuit is designed and connected at the output. The step load change is applied at regular intervals as desired using the GPIO pin configured as a digital output. This signal is used to switch (Power MOSFET IRF7103PbF) as illustrated in figure 6.3. By using different resistor values (R_1, R_2, R_3, and R_4) and appropriately control the switching time, the load seen by the power converter can be changed from 50% to 80% of the full load, as desired for the test.

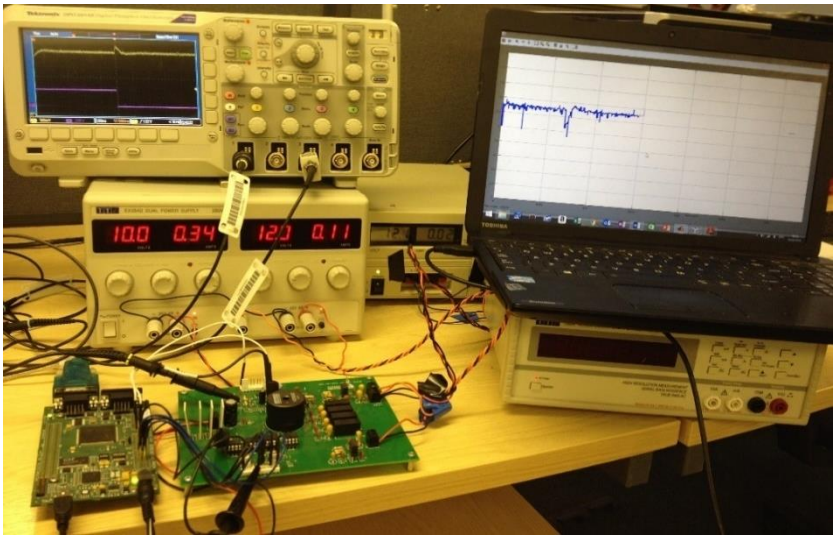


Figure 6.2 Hardware overview of the experimental setup

The parameters of the prototype synchronous buck converter are listed in Table 6.1. To test the presented configuration, figures 6.4(a) shows the PWM generated and the converter output voltage in the open loop with a 33% duty cycle. Here, complementary PWM signals are generated with a 1 microsecond dead band configured to avoid switching both MOSFETS *On* at the same time as shown in figure 6.4(b).

Table 6.1 Parameters for the experimental synchronous buck converter

Symbol description	Value
V_{in}: Input voltage	10 V
L: output inductor	220 μH
C: output capacitor	330 μF
R_C: equivalent series resistor	25 mΩ
R_L: inductor series resistance	63 mΩ
R_o: load resistance	5 Ω
T_s: switching and sampling time	50 μs

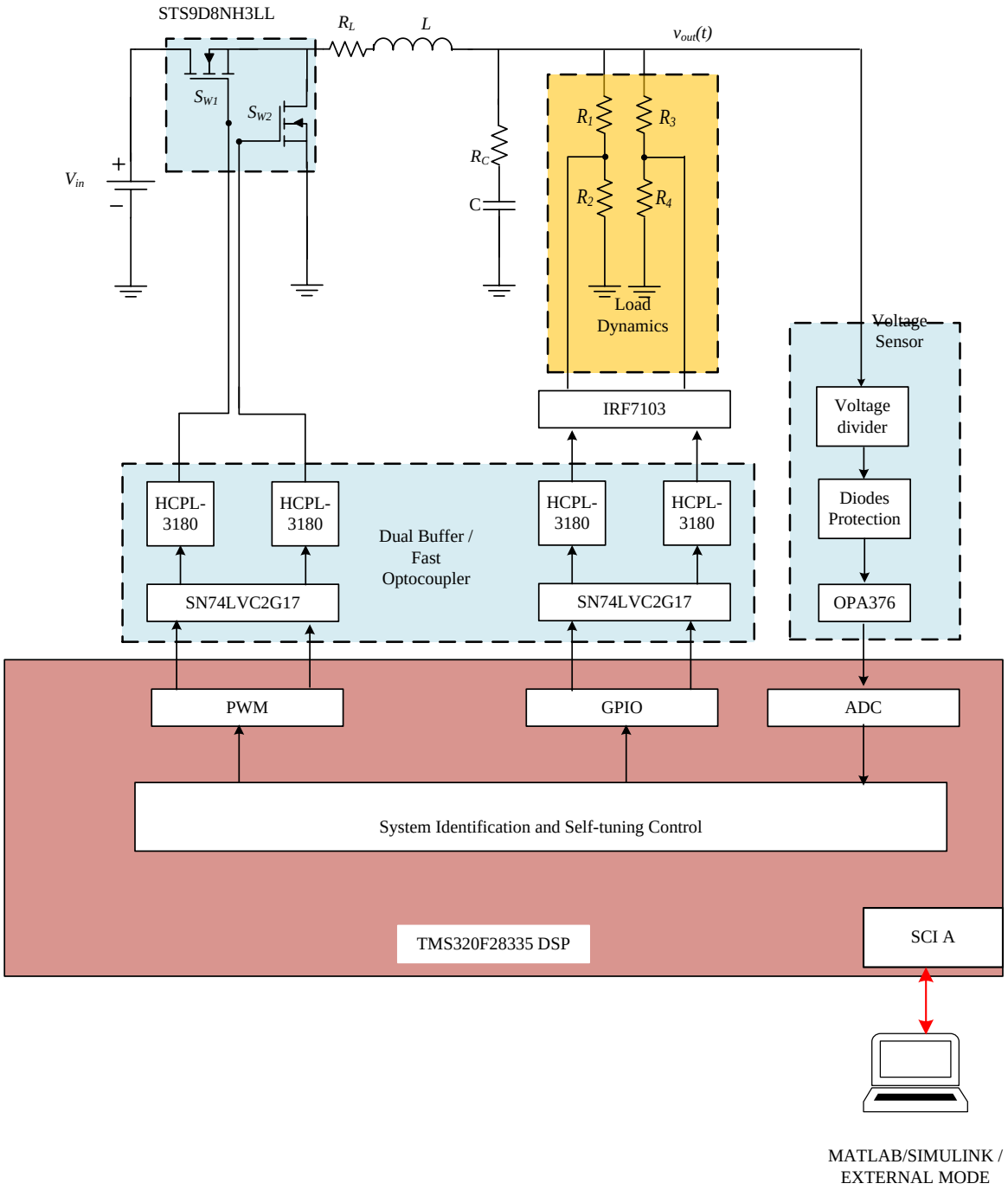
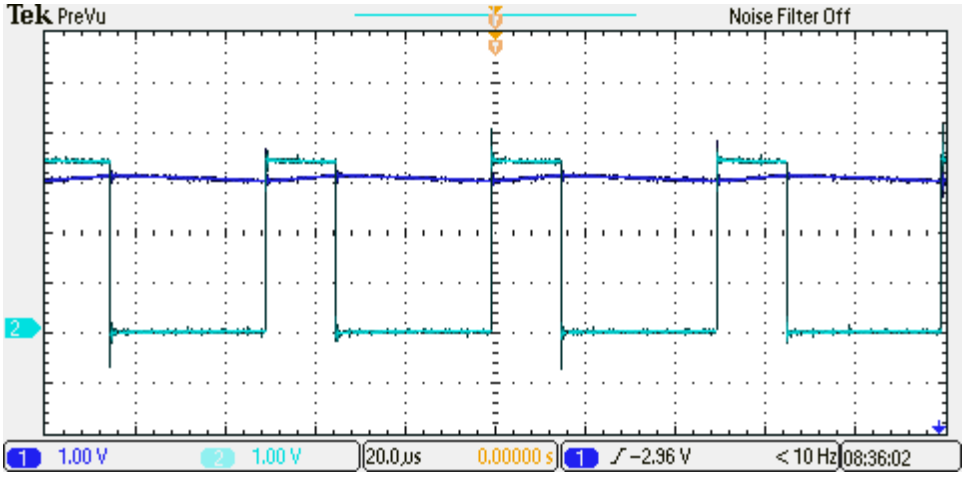
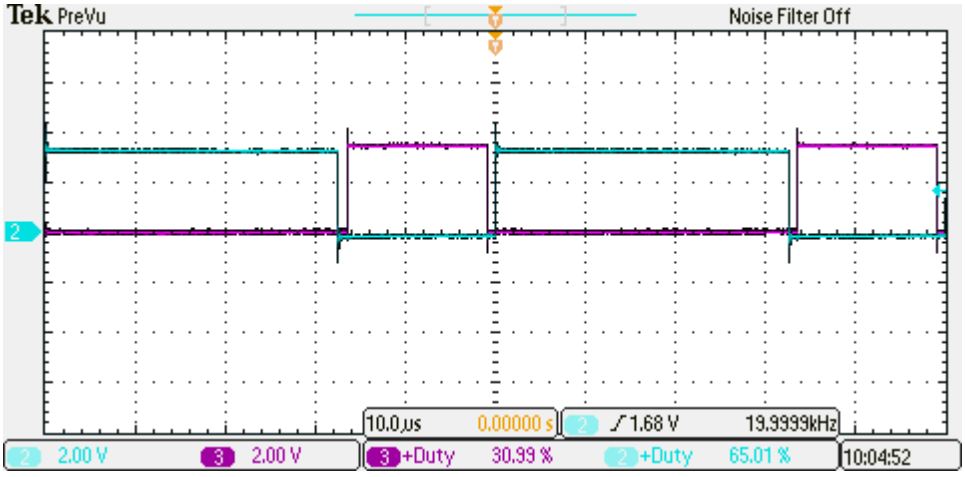


Figure 6.3 Block diagram of digitally voltage-controlled synchronous DC-DC buck converter



(a)



(b)

Figure 6.4 Generated PWM waveforms in the open loop test: a. output voltage with duty ratio 33%; b. the primary and secondary gate signals with 1µs dead time in a symmetrical case

6.5 Real-Time Parameter Estimation of DC-DC Converters using a Self-tuned Kalman Filter/ Experimental Validation

To experimentally validate the previously demonstrated advantages of the KF over the ERLS algorithm in Chapter 4, this section introduces a complete real-time implementation of both algorithms. Using the code development tool described in section 6.3, the same identification procedure was outlined in section 4.7 is followed here and implemented in the TMS320F28335 DSP. This included, generating the PRBS signal, enabling the identification algorithm for a specific period of time (20 ms), and implementing a digital PID controller designed based on the pole placement technique. In the field of system identification, it is

recommended to investigate the suitability of the data being used and the selected model structure in order to proceed to the next step and to use the identification results for control design. Therefore, an off-line test is carried out first here. This test started via injecting a PRBS signal into the duty cycle to perturb the output voltage as shown in figure 6.5. A small amplitude signal is selected for the excitation signal to keep the perturbation within 5% of the nominal output voltage during the identification procedure; it then reverted back to normal operation as depicted in figure 6.5.

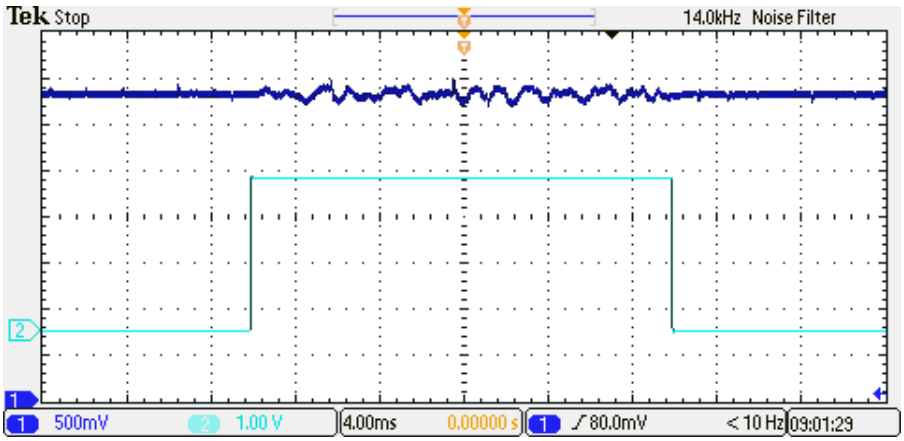


Figure 6.5 Experimental output voltage during identification process

Using the data logging feature in Simulink External mode, the output voltage and the control signal during the excitation period are both sampled at 20 kHz and exported to the MATLAB workspace. After the full sequence is recorded, a post-processing step is applied to filter the raw data and remove offsets. For filtering, a simple four-tap moving average (MA) filter is applied to smooth the input and output data by removing unwanted high frequency measurement noise. This filter type is selected due to its simple structure and ease of DSP implementation. Figure 6.6 highlights the filtered output voltage and duty cycle data from the DC-DC converter during the identification process. In the applied recursive algorithms, the data vector components are assumed to be zero mean values. Therefore, each sample is subtracted from the mean value to remove the offsets and to obtain a raw data with zero mean value. In DC-DC SMPC applications, the mean values of the regulated output voltage and the average duty-cycle ratio are known. Thus, they can be directly used to perform offset removal at each time iteration. The obtained signals are then fed to the KF algorithm to estimate the coefficients of the adaptive filter cycle-by-cycle and hence minimise the prediction error signal. It is worth

noting that the initial values of the KF algorithm is kept the same as those used in the simulation step.

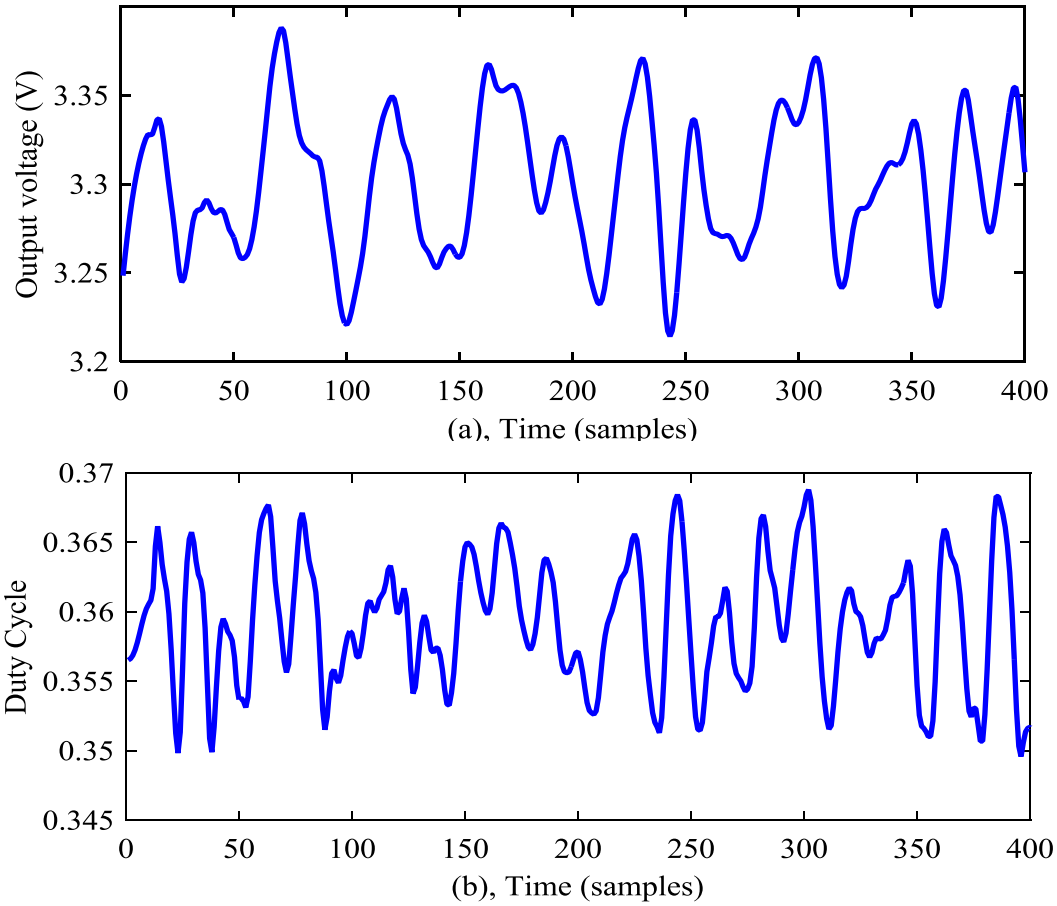


Figure 6.6. Experimental filtered data sampled at 20 kHz: a. output voltage; b. duty cycle

Figure 6.7 shows the off-line estimation results, which confirm that the selected ARX model structure is suitable to describe the dynamics of the converter. Furthermore, the simple four-tap MA filter is sufficient to carry out the filtering task for a successful parameter estimation process. The results show very good agreement with the original simulation results illustrated in figure 4.8. To validate the applied identification procedure, different real-time data sets have been collected and used to estimate the discrete transfer function of the DC-DC buck converter. Comparable results have been obtained, which motivated the next step that aimed to perform the entire identification process on the DSP in real-time without any remote intermediate post-processing analysis unlike a significant proportion of the existing literature. Figure 6.8 shows the output voltage during the real-time identification process, which is enabled for 20 ms, while the PRBS signal is injected into the duty cycle for 10 ms only in order to examine the stability of both algorithms without the perturbation signal.

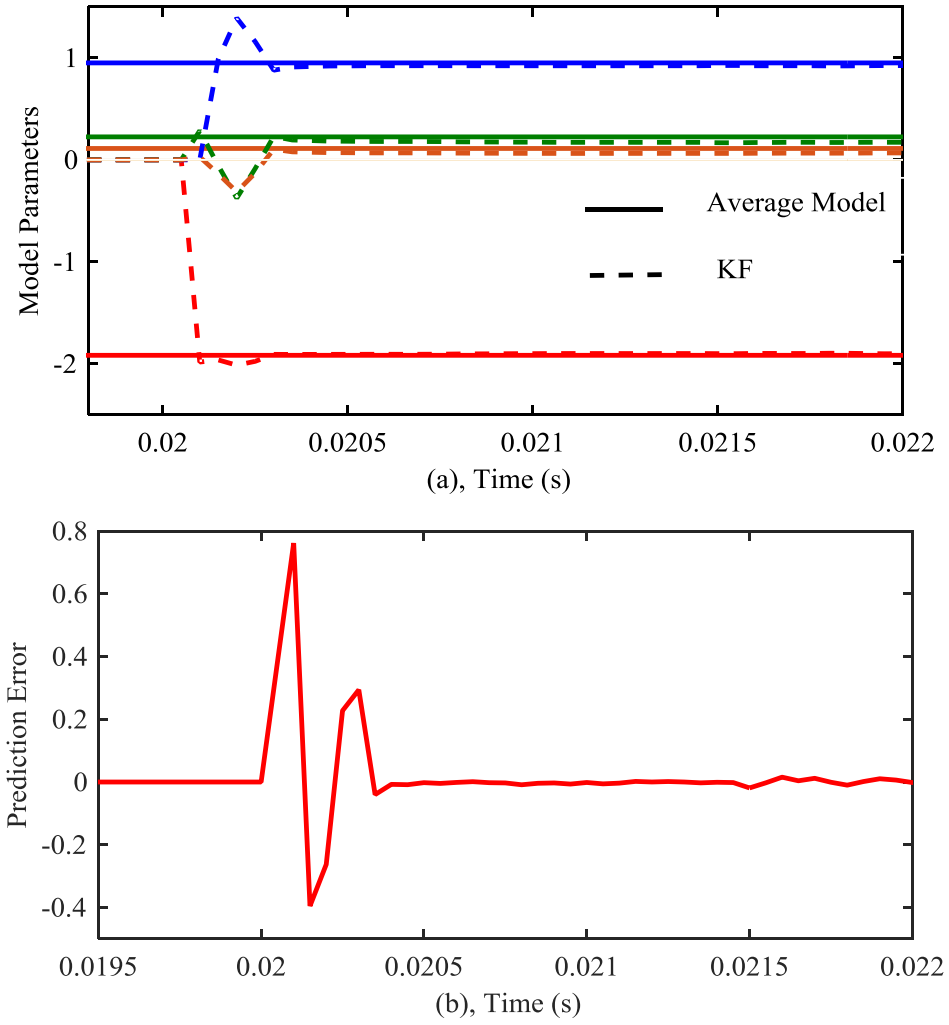


Figure 6.7 Off-line parameter estimation using experimental data: a. model parameters; b. prediction error

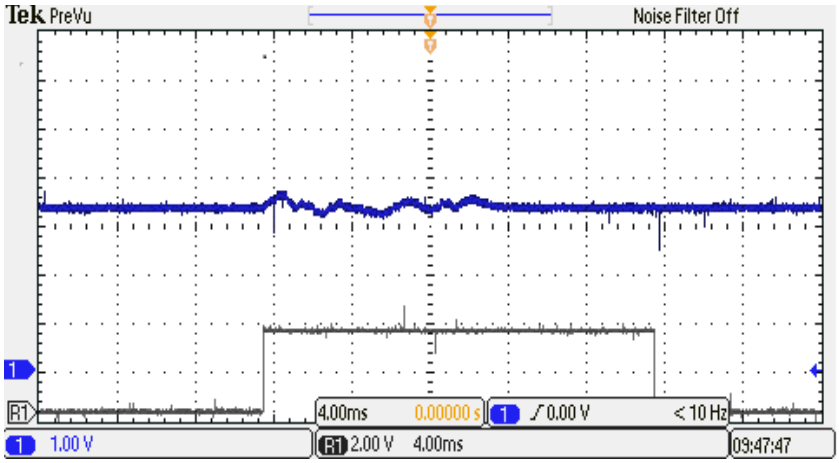


Figure 6.8 Experimental output voltage during identification process with PRBS signal disabled after 10 ms

6.5.1 *Real-Time Results for KF and ERLS*

Similar to the simulation procedure, the ERLS with forgetting factor λ= 0.95 is investigated. As shown in figure 6.9, the ERLS required around 5 samples (0.25 ms at sampling time 50 µs) to converge to the steady-state value for denominator coefficients (a_1, a_2) with an accuracy range ±7% (figure 6.9(a)), while the numerator taps takes longer to converge (around 1ms), as there is a clear offset in the final estimation (figure 6.9(b)). The limited accuracy of the ERLS estimator during the excitation period can be clearly demonstrated via the estimation error signal, as illustrated in figure 6.9(c). Consequently, if the estimated coefficients are used for health monitoring purposes, as introduced in a previous study [1], inaccurate decisions may be taken in terms of predicting the health or age of the circuit components. In comparison with the simulation results presented earlier in figure 4.8, the estimation accuracy of the ERLS estimator is highly affected by measurement noise in the experimental implementation.

To study the impact of the excitation signal on the estimation results, the PRBS signal is actively disabled after 10 ms, as shown in figure 6.8. Due to the scaler-forgetting factor used in ERLS, the estimated parameters start to deviate from steady state, which agrees with the simulation results in figure 4.13. This phenomenon is known as estimator wind-up, where the error covariance matrix grows exponentially and yields a high adaptation gain applied in the correction step. Therefore, the ERLS is not a reliable estimator if a self-tuning controller is desired. Hence, in direct digital control design such as the pole placement approach or the Bányász/Keviczky PID controller, the estimation results are fed to the controller directly, which may cause the system to be unstable since the values of (b_1, b_2) are not accurate

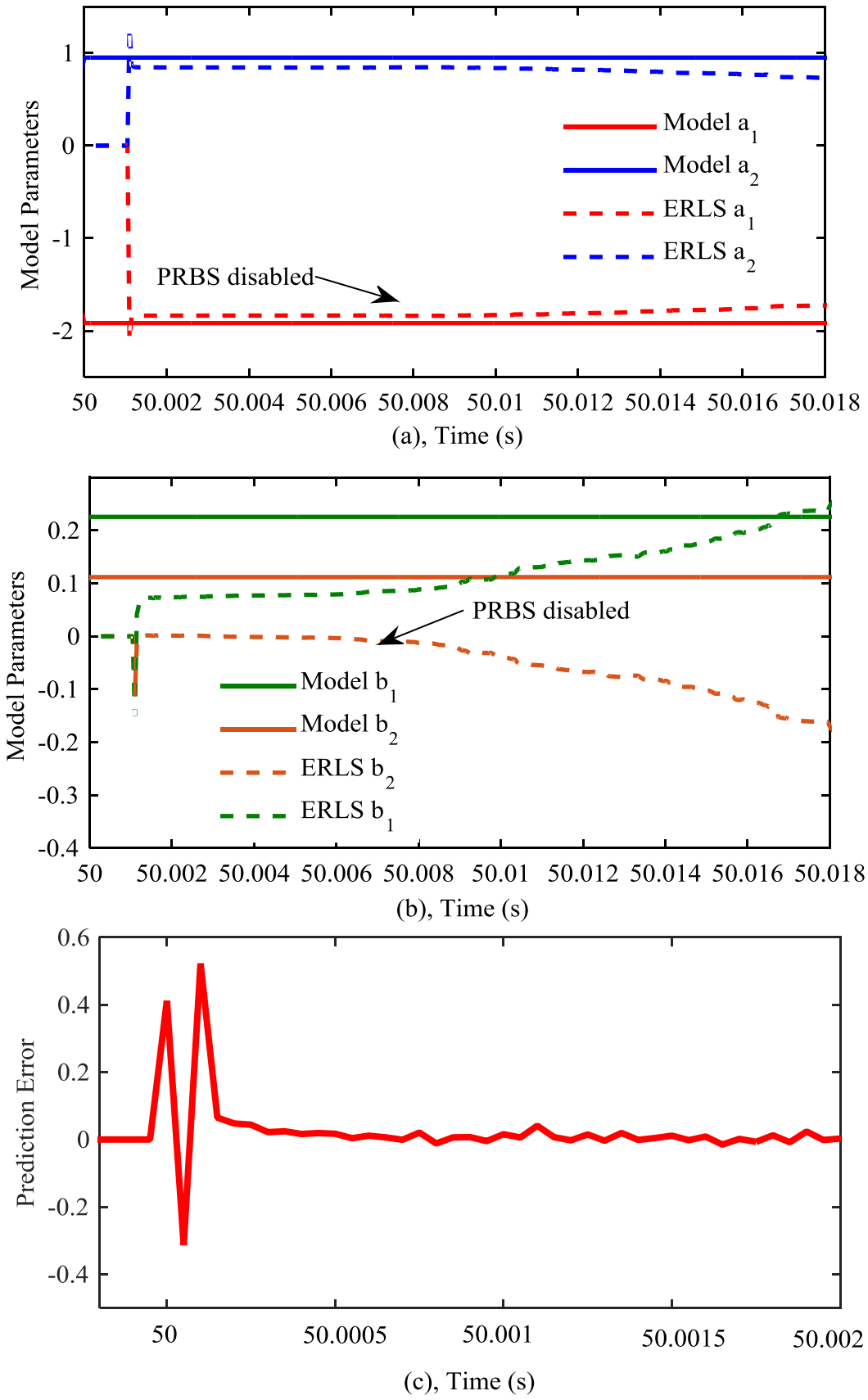


Figure 6.9 Real-time parameter estimation results using ERLS: a. denominator coefficients; b. numerator coefficients; c. steady state prediction error

The proposed KF algorithm is also evaluated and the estimated poles and zeroes parameters compared with the average model parameters with a resistive load equal to 5 Ω. In figure 6.10, the parameters a_1, a_2 converge to steady state-values in less than 0.15 ms, which is faster than the ERLS method with less over/undershoot, and with a 0.3% estimation error. This confirms the simulation results depicted in figure 4.8. In comparison with the ERLS, the parameters b_1, b_2 are estimated within a similar period of time, but with enhanced accuracy. Importantly, the execution time of the proposed KF, measured in real time using Code Composer Studio, is only 3 μs longer than the ERLS. Similarly to ERLS, the stability of the KF is examined when the PRBS signal is disabled, as illustrated in figure 6.10, and at 50.01s, the KF has the ability to produce a smooth and stable estimation with no effect of estimator wind-up. Therefore, the results highlight stable self-tuning compensation since the zero coefficients do not fluctuate and stay very close to the pre-calculated ones. In addition, the observed prediction error (figure 6.10(c)) confirms the advantages of the KF over the ERLS in terms of accuracy and improved convergence speed for transfer function estimation. The results obtained for both algorithms investigated are summarised in Table 6.2, which demonstrates that the KF outperforms ERLS in terms of accuracy and convergence time, though with a small extra execution time required due to the tuning step outlined in section 4.5.

Table 6.2 Steady state parameter estimation comparison between ERLS and KF

Parameter	KF	ERLS	MODEL
a_1	-1.922	-1.822	-1.913
a_2	0.925	0.842	0.946
b_1	0.161	0.087	0.2259
b_2	0.0991	-0.00573	0.1118
Convergence time	0.15 ms	0.25 ms	
Computational time per iteration	37 μs	33 μs	

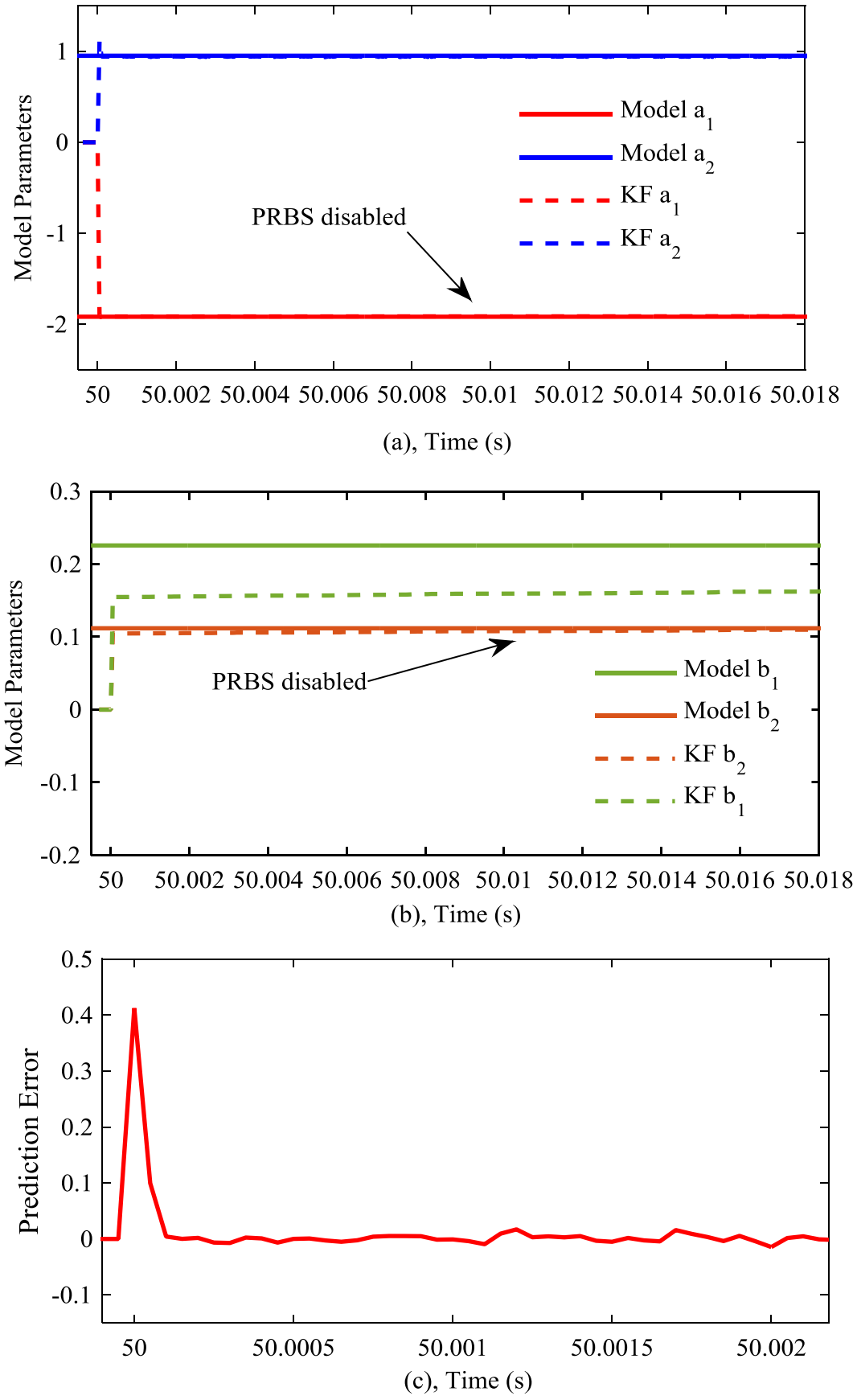


Figure 6.10 Real-time parameter estimation results using KF: a. denominator coefficients; b. numerator coefficients; c. steady state prediction error

6.5.2 ***Model Validation***

From the estimation results for both algorithms, it can be seen that the prediction error converges to zero in both cases with a small difference in the convergence rate. This theoretically means that the ERLS and the KF have the same estimation results, which is not actually the case as highlighted in the results. Here, accuracy is judged based on the derived average model known to the designer. However, this knowledge cannot always be provided or the actual parameters may change over time due to ageing or other reasons. Therefore, a validation step is introduced to show which estimated model is suitable to describe the dynamic behaviour of the converter. This test is accomplished by studying the correlation between the residuals and past inputs for *N* samples, as indicated in (6.2).

$$R_{eu}^{N}(\tau) = \frac{1}{N}\sum_{k=1}^{N} e(k)\,u(k-\tau) \tag{6.2}$$

From the cross-correlation test depicted in figure 6.11, it can be seen that a small cross-correlation is observed when the residuals of the KF are used, while a higher cross-correlation is recorded in case of the ERLS residuals. Therefore, the prediction error in the KF is considered as white and no further information is required to improve the estimated model. On the other hand, the estimated model using the ERLS is not suitable for identification purposes as it is affected by measurement noise.

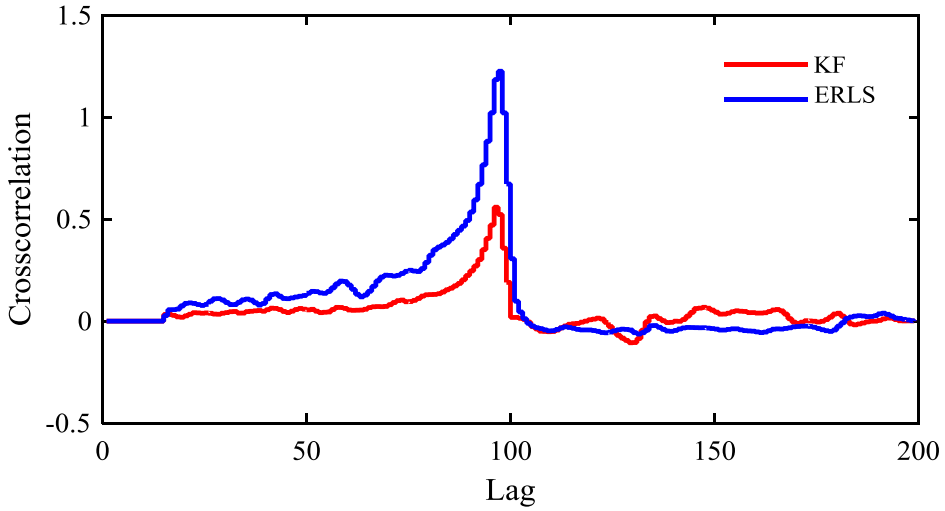


Figure 6.11 Residuals, cross-correlation function

6.5.3 ***Abrupt Load Change / Real-Time Results***

Similar to the simulation test, a wide and abrupt load change is applied to further investigate the performance of the proposed self-tuned KF. Figure 6.12 shows the dynamic response of the output voltage when the load is changed from 5 Ω to 1 Ω at 50.015 s. As confirmed previously, the KF can provide good estimation performance without any perturbation in the observed data, and this can be clearly seen from the recorded output voltage during the identification procedure figure 6.12, where no excitation signal is injected. This scenario is applied deliberately because in the case of the ERLS the estimated parameters deviate immediately once the PRBS is disabled, and so if the load changed after this instant the ERLS would not be able to detect the new variation and another perturbation period is required to perform the estimation process. Therefore, to provide a fair comparison, a PRBS signal is injected before the step change is applied to investigate the performance of the tracking capability of the ERLS in response to load variation. On the other hand, the KF estimator stays alert for a longer time, and hence no perturbation is required to detect the load change.

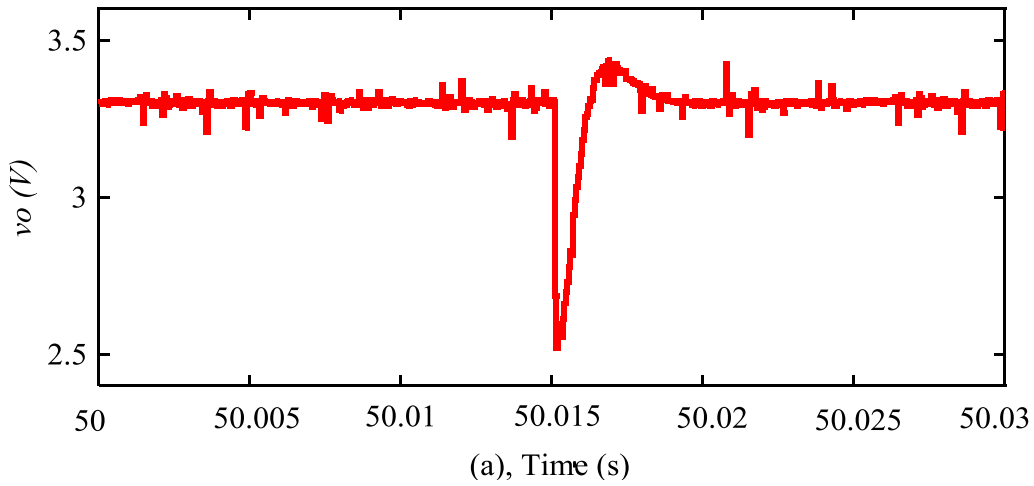


Figure 6.12 Output voltage recorded on the DSP during a step load change from 5 Ω to 1 Ω at 50.015 s

Figure 6.13(a), shows the KF estimation results, with the transfer function poles accurately estimated before and after the load change with a convergence time less than 1 ms, and with a 0.4% estimation error. In contrast, the ERLS estimation has a clear offset during the steady state, which improved after the load change as illustrated in figure 6.13(b) achieving a 1.1% estimation error. This behaviour confirms that the ERLS estimator requires a large perturbation signal to provide accurate and reliable estimation. In line with the simulation

procedure, the numerator parameters are not illustrated here due to the small effect of the load change, which can be ignored according to the computed transfer function 4.33 and 4.34.

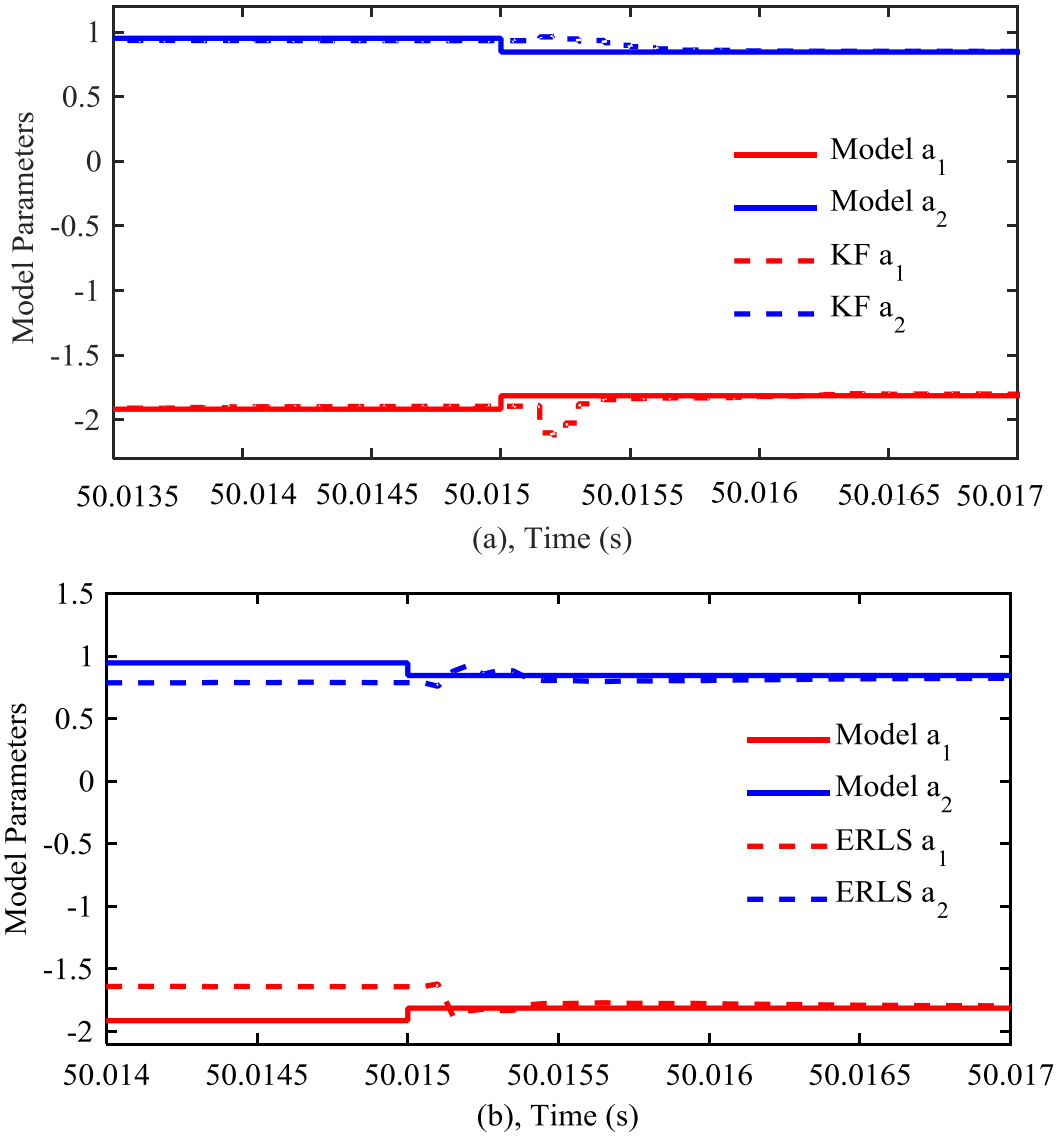


Figure 6.13. Real-time parameters estimation during a step load change from 5 Ω to 1 Ω at 50.015 s: a. KF estimation, b. ERLS estimation

For more insight into the performance of both algorithms in tracking time-varying parameters, the behaviour of the experimental adaptation gain is recorded in steady state and during the load change for the self-tuned KF and for the ERLS as illustrated in figure 6.14. As the same tuning method outlined in section 4.5 is applied in the experimental validation, the real-time estimation obtained shows excellent agreement with the original simulation results in figures 4.11 and figure 4.12. With the assigned Kalman gain elements K_1 for a_1 and K_2 for a_2

varying with different rates in the correction step, the proposed self-tuned KF can provide a reliable and accurate estimation even for fast and significant parameter variations. For the ERLS algorithm, the experimental validation demonstrates that this algorithm requires a significant perturbation such as the applied load step in order to produce accurate and stable estimation. Furthermore, the experimental adaptation gain behaves as expected since the same magnitude with different directions are given during the correction step for both coefficients a_1 and a_2 due to the single forgetting factor scheme. This result clearly shows that the KF algorithm outperforms the classical ERLS in terms of achieving smaller estimation error with a rapid convergence rate in response to abrupt load change.

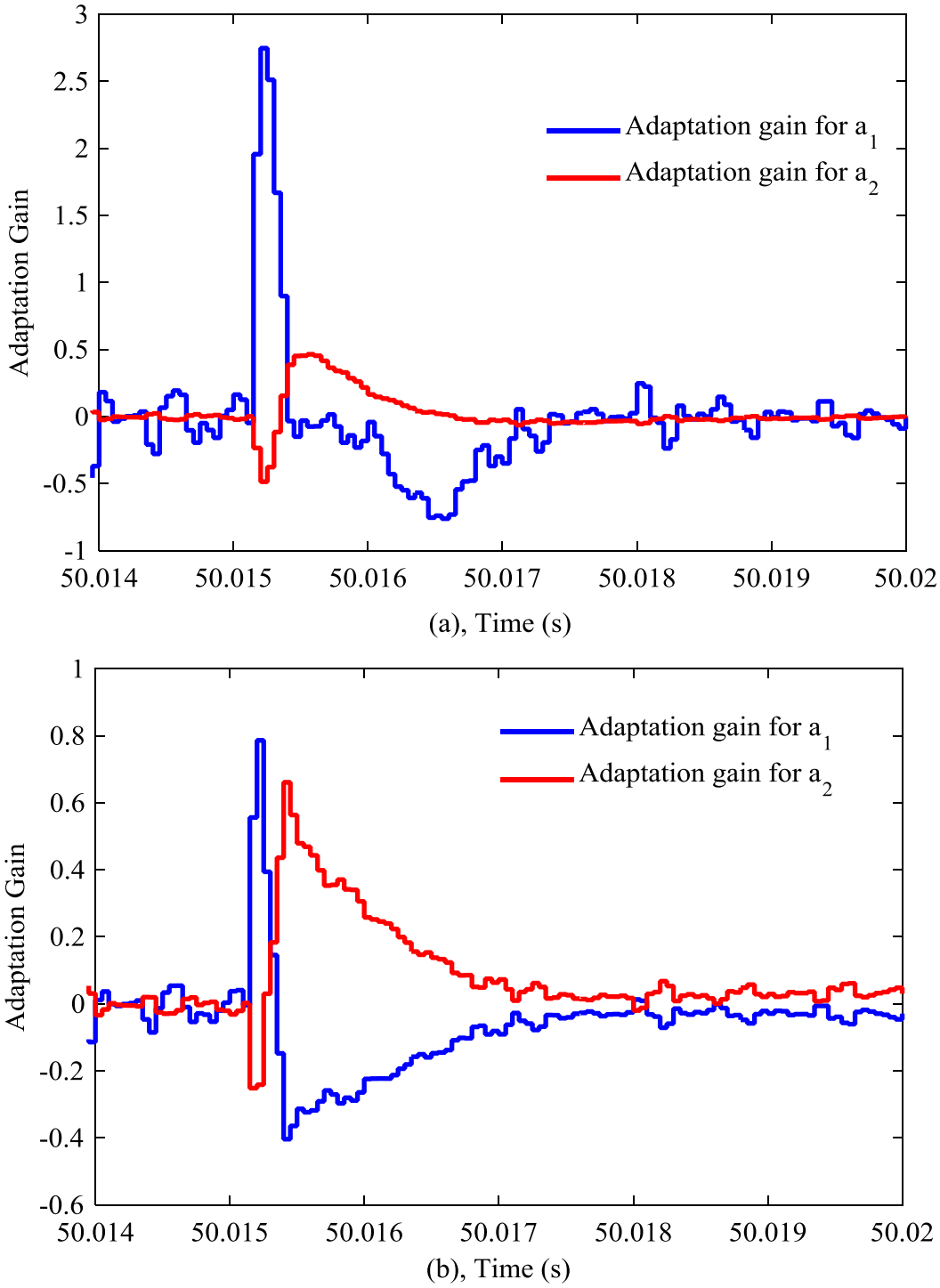


Figure 6.14 Adaptation gain behaviour during abrupt load change: a. KF; b. ERLS

6.6 Experimental validation of the STC Design using the Developed M-Max PUKF

This section presents the practical validation of the designed STC based on the developed M-Max PUKF configured for parameter estimation. The validation procedure started by regulating the output voltage at 3.3 V using a digital PID voltage controller. The PID gains are computed using the well-recognised pole-placement technique as previously presented in Section 2.10.1. This approach is usually adopted if a direct digital control design is required. Therefore, it is introduced here to serve as benchmark for evaluating the Bányász/Keviczky PID controller based on the M-Max PUKF.

Firstly, the converter operates in steady state and a practical implementation of the simulation procedure in section 5.7 is conducted on the DSP. This includes, the real-time implementation of the full KF, M-Max PUKF, and the on-line design of the STC. Initially, the full update KF is activated at 50 s to identify the coefficients of the discrete transfer function $[a_1, a_2, b_1, b_2]$ as shown in figure 6.10. Once full estimation is accomplished, the developed M-Max PUKF is enabled at 50.01 s to estimate the selected subset of the adaptive filter coefficients $[a_1, a_2]$.

6.6.1 *Parameter Estimation Using PUKF/ Real-Time Results*

Figure 6.15(a) illustrates the estimation results using the developed M-Max PUKF. Apart from the small decrease in accuracy of coefficient a_2 , the selected parameters a_1, a_2 converge to steady state-values in less than 0.5 ms which demonstrates excellent agreement with the simulation results shown in figure 5.6(a), thus confirming the successful real-time implementation of the proposed M-Max PU KF as a reliable estimator. In order to update the full parameter vector, a periodic PUKF is enabled at 100 s to estimate the less important coefficients $[b_1, b_2]$ as shown in figure 6.15(b) results comparable with those of the full estimator in terms of accuracy are achieved, while a longer convergence time in about 3 ms is observed due to their small error contribution. Importantly, the execution time of the proposed PUKF, measured in real time using Code Composer Studio, is 18 μs which indicates around 50% complexity reduction compared to the full KF investigated in section 6.5.1.

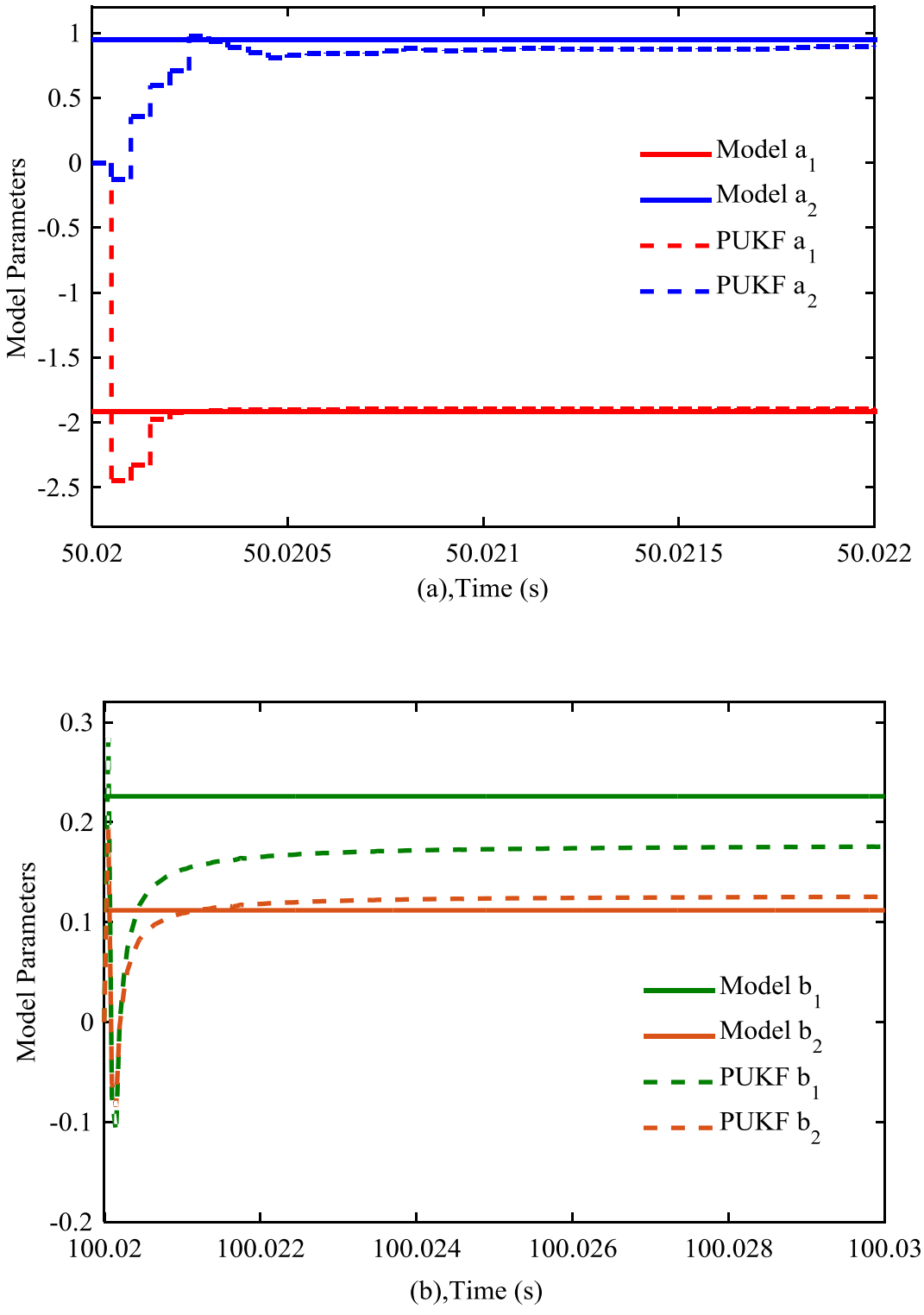
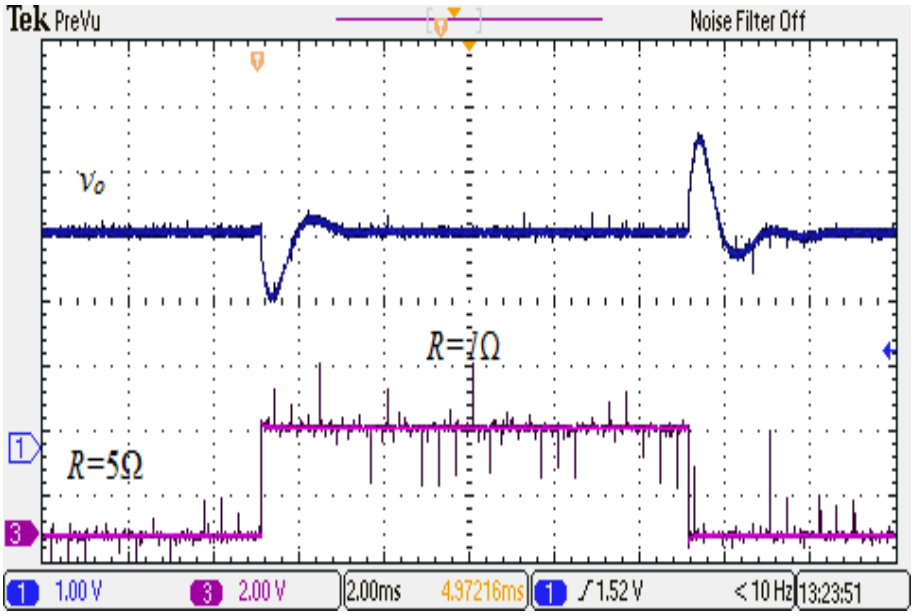


Figure 6.15 Real-time parameter estimation results: a. denominator coefficients using M-Max PUKF; b. numerator coefficients using periodic PU KF

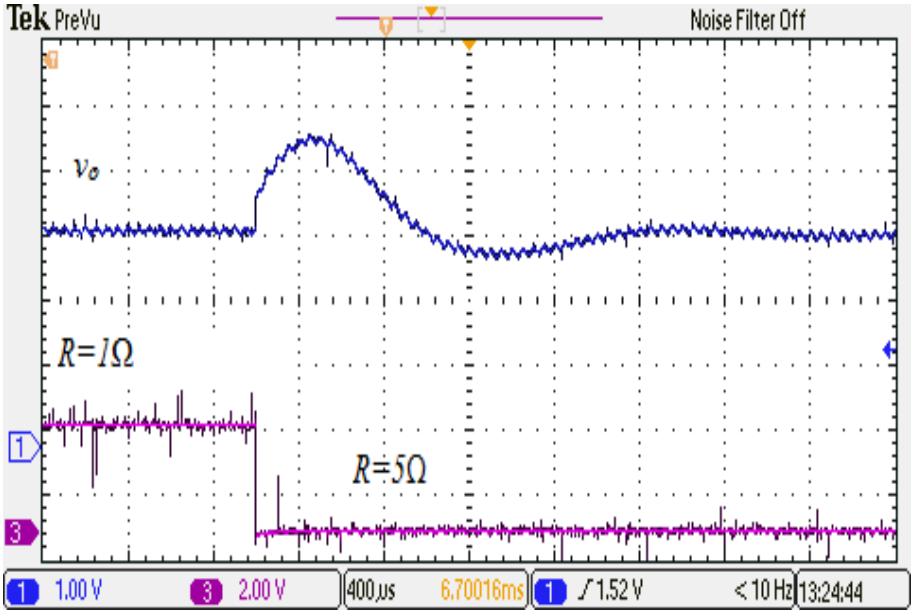
6.6.2 *Improved Transient Response with Proposed STC*

Once the discrete transfer function is fully estimated, the self-tuning Bányász/Keviczky PID controller is then activated to regulate the output voltage at 3.3 V. As an important factor in assessing the designed STC, the converter is subjected to a step load change to investigate the dynamic performance. This test is conducted for a significant load change between 5 Ω to 1 Ω every 10 ms. To evaluate the the transient characteristics of the designed STC, the same test is applied on the buck converter controlled using the well-recognised pole-placement technique.

The waveforms in figures 6.16 and 6.17 show a comparison of the load transient responses of the pole-placement PID controller and the designed explicit STC scheme respectively. In figure 6.16, it can be seen that the output voltage transient shows significant oscillatory behaviour at the points of load change. Here the output voltage recovers to 3.3 V in 1.8 ms with 48% overshoot. In contrast, the self-tuning improves the dynamic characteristics of the controller (figure 6.17), resulting in a significantly faster recovery time in 1.2 ms with lower transient overshoot and no voltage drops observed. Importantly, the execution time of both controller algorithms is measured in real time using Code Composer Studio. This shows that the classical pole-placement controller is executed in 9.5 μs whereas the proposed STC takes 2 μs to compute the control action. This means the whole STC scheme proposed here requires only 20 μs to be executed each iteration on the DSP. As a result, the switching frequency can be increased or the entire STC can be implemented in lower cost microcontroller hardware. It is worth noting that the switching frequency effect seen on the experimental waveforms is due to the common mode noise on the oscilloscope probe.

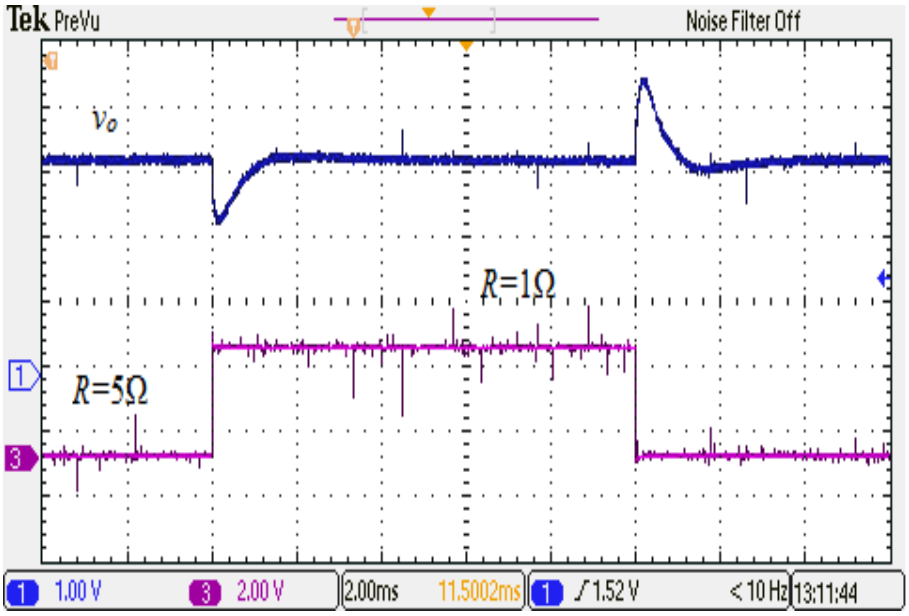


(a)



(b)

Figure 6.16 Transient response of the pole-placement PID controller with abrupt load change between 5Ω and 1Ω: a. 2 ms/div: showing two transient changes; b. 400 µs/div: "zoom-in"on second transient



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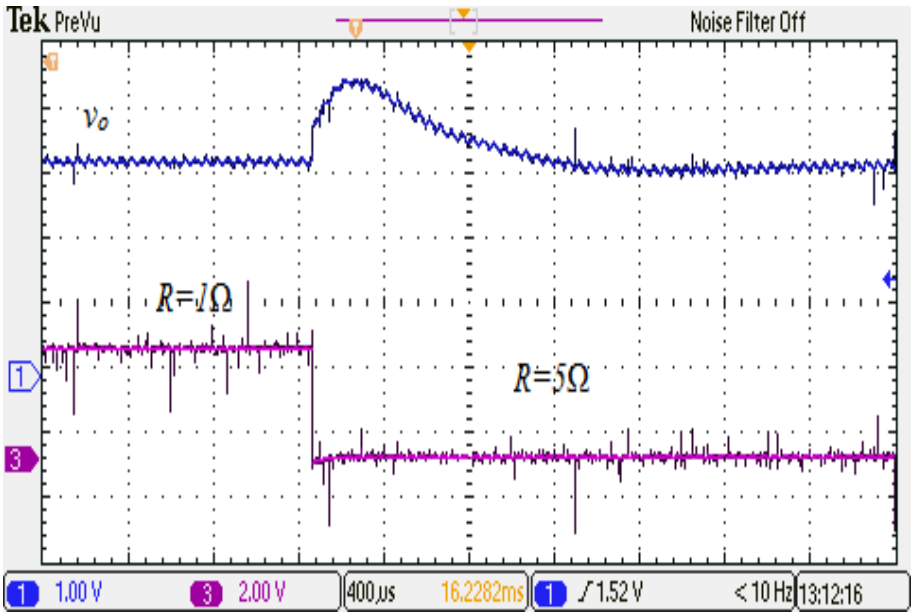

(b)

Figure 6.17 Transient response of the explicit STC with abrupt load change between 5 Ω and 1 Ω: a. 2 ms/div showing two transient changes; b. 400 µs/div "zoom-in" on second transient

6.7 Chapter Summary

This chapter has presented the experimental validation of the KF identification algorithm introduced in Chapter 4 and the proposed explicit STC scheme based on the PUKF illustrated in Chapter 5. A complete real-time implementation was conducted on a DSP to verify the performance of both algorithms online. The experimental results of the system identification method are in very good agreement with the simulation results illustrated in Chapter 4, indicating the practicality of the proposed algorithm for real-time application. Moreover, the robustness and tracking capability of the estimator has been investigated, and the results validate that the KF estimator is more reliable than the conventional ERLS algorithm in tracking time-varying parameters and in estimation stability. In addition, the proposed M-Max PUKF has been successfully implemented and employed in a real-time explicit STC scheme. The experimental results have confirmed the viability of integrating the PUKF with a low complexity control scheme such as the Bányász/Keviczky PID controller method in real-time. The final set of experimental results demonstrates an enhancement in the transient response attained with the explicit STC scheme compared to the conventional PID controller designed based on a pre-calculated average model.

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Chapter 7 Conclusion and Future Work

7.1 Conclusion

To achieve a high performance control of modern SMPCs, using direct digital design techniques, an accurate discrete model of the converter is necessary. In order to acquire this model, a parameter estimation scheme is involved. This combination is known as explicit self-tuning control strategy, where the discrete model of the converter is estimated from online measured input/output data using a recursive identification algorithm, and then a controller design method is implemented to compute the control signal based on the acquired knowledge from the estimation step. Accordingly, the recursive algorithm plays a vital role in this synthesis, as it must be able to provide high levels of accuracy and/or estimation speed in response to any unpredicted behaviour such as sudden load variations, components aging, noise, and unpredictable changes in operating mode. However, the algorithm reliability in providing accurate estimation and the computational cost are the major concerns in the explicit STC paradigm.

For online parametric identification, the classical ERLS algorithm is widely applied due to its accurate estimation, fast convergence speed, and small prediction error. However, in practical applications such as SMPCs, the estimation accuracy of the ERLS technique is highly affected by measurement noise, which reduces the reliability of the estimation results when used in explicit STC scheme, or for condition monitoring purpose. In addition, the tracking capability is controlled by means of single forgetting factor. Typically, this technique applies the same adaptation gain to all parameters regardless of their rate of variation in respond to unpredicted behaviour such as a sudden load change in SMPCs. As a result, the estimation of coefficients with small values will suffer from slow convergence speed and higher estimation error. Furthermore, the ERLS algorithm requires injecting a frequency rich signal to enhance the estimation accuracy and prevent estimator wind up due to an exponential growth of the adaptation gain matrix. This necessitates keeping the output voltage perturbed for long periods or resetting the estimator periodically, which can lead to some abrupt changes not being observed.

To attain a stable and accurate steady-state estimation with short perturbation period and improved tracking capability for time-varying parameters, the error covariance matrix must be updated using a different approach to add more freedom to the adaptive algorithm when calculating the adaption gain. In this thesis, a research contribution is made by introducing a new parametric system identification method, based on the KF approach to overcome the highlighted limitations of the ERLS algorithm. A further research contribution of this thesis is incorporating a new state-of-the-art tuning method for the process covariance matrix to optimise convergence speed and allow the estimator to track time varying parameters. The self-tuned KF technique has the potential for use in real time system identification and adaptive control systems for power electronic applications, such as switch mode power supplies.

Here, the mathematical description of the proposed algorithm is presented, and the algorithm is fully validated in simulation using MATLAB/SIMULINK, and experimentally using a Texas Instruments TMS320F28335 microcontroller platform and synchronous step down DC-DC converter. In this thesis, unlike a significant proportion of existing literature, the entire system identification and closed loop control process is seamlessly implemented in real-time hardware, without any remote intermediate post processing analysis. Simulation and experimental results, show that the proposed self-tuned KF can accurately identify the discrete coefficients of the DC-DC converter. Furthermore, the estimator convergence time is significantly shorter compared to many other schemes, such as the classical ERLS method. The advantage of this has been successfully validated via an abrupt step change in load. The performance of the Kalman filter is also tested without a perturbation signal, and the results obtained prove that the covariance matrix update scheme keeps the estimator stable and responsive for longer periods of time. Furthermore, and important from a practical perspective, the effect of estimator wind up is reduced.

The results and conclusions of this work have successfully been published in the following journal and international conference papers:

1. **M. Ahmeid,** M. Armstrong, S. Gadoue, M. Algreer, and P. Missailidis, "Real- Time Parameter Estimation of DC-DC Converters using a Self-tuned Kalman Filter," IEEE Transactions on Power Electronics, vol. PP, pp. 1-1, 2016.

2. **M. Ahmeid**, M. Armstrong, S. Gadoue, and P. Missailidis, "Parameter estimation of a DC-DC converter using a Kalman Filter approach," in Power Electronics, Machines and Drives (PEMD 2014), 7th IET International Conference on, 2014, pp. 1-6.

The second major contribution of this thesis is the computational complexity reduction of the proposed self-tuned KF by means of using a partial update scheme. This means, instead of updating all of the $N \times 1$ coefficients in the parameter vector, the partial-update method only updates $M \times 1$ coefficients, where $M < N$. The selection of the subset to be updated is based on the data vector analysis or called M-Max partial update method. By adopting this technique in the proposed self-tuned KF algorithm, a significant complexity reduction is achieved as the number of arithmetic operations are reduced, more specifically the computation of adaptation gains and covariance updates. These two steps constitute the bottleneck of the recursive algorithms since elaborate matrix multiplications are required to update the parameters at every iteration step.

In DC-DC buck converter, the denominator coefficients $[a_1, a_2]$ are appointed as the more important parameters according to the data vector analysis and the importance of system poles in terms of stability and control design. To successfully implement the M-Max PUKF, the full KF is activated for short time at the beginning of the identification procedure to estimate all the transfer function coefficients $[a_1, a_2, b_1, b_2]$. Then the M-Max PUKF is activated for the rest of the identification process to update the denominator coefficients $[a_1, a_2]$ at each time iteration for the rest of the identification procedure. As a result, the M-Max PUKF achieves around 50% computational complexity reduction in comparison with the full version described in the first contribution. In addition to the development of low complexity estimation algorithm, the explicit STC scheme is constructed using simple and robust control design method suitable for real time power electronic applications. This algebraic control method is called Bányász Keviczky PID controller, which uses only the discrete time model to calculate the controller elements with a substantial reduction in required number of arithmetic operations in comparison with the well-known pole placement technique. Simulation and experimental results, based upon a prototype synchronous DC-DC buck converter controlled by Texas Instruments TMS320F28335 DSP, show that the viability of adopting PU method in real-time parameter estimation for DC-DC converters. The developed M-Max PUKF provides fast convergence speed, small prediction error, and accurate parametric estimation very close to the full KF. In

addition, the results confirmed the feasibility of integrating the PUKF with low complexity control scheme such as Bányász/Keviczky PID controller method in real-time. Furthermore, the final set of experimental results demonstrate an enhancement in the overall dynamic performance of the closed loop control system compared to the conventional PID controller designed based on a pre-calculated average model. Identical to the first contribution, the identification procedure using full KF, PUKF, and controller design is completely executed on real-time hardware, without any remote intermediate post processing analysis.

The results and conclusions of this work have successfully been submitted in the following journal paper:

1. **M. Ahmeid**, M. Armstrong, S. Gadoue, M. Algreer, and P. Missailidis "Computationally Efficient Self-Tuning Controller for DC-DC Switch Mode Power Converters Based on Partial Update Kalman Filter", under review in the IEEE Transactions on Power Electronics.

7.2 Future Work

This thesis has focused on real-time implementation of parametric system identification techniques and employing them in explicit STC scheme for a buck DC-DC SMPC. The developed methods can be further investigated on other power converter topologies to demonstrate and investigate the overall performance in more complicated systems and other converter topologies. In terms of recursive algorithms, it may be worth investigating alternative tuning methods with forgetting factor strategies, and to study in detail the effect of the selected initial values of the error covariance matrix in terms of considering off-diagonal elements. Furthermore, the real-time implementation could include a validation step based on residual analysis to produce a complete identification procedure ready for DSP implementation.

The proposed STC structure can be expanded to include health monitoring schemes. This can be achieved by means of developing an efficient technique to extract the actual component values from the estimated discrete transfer function.

It will also be interesting to investigate code development tools for applying more complicated algorithms such as non-parametric system identification methods. This kind of

implementation can exploit more powerful DSPs or FPGAs to improve their computation capability.

Appendix A. Derivation of RLS Algorithm Based on Matrix Inversion Lemma

In order to rewrite the least squares solution denoted in (4.7) in a recursive form, the matrix $\Phi\Phi^T$ has to be non-singular for all observations k and the $N \times N$ covariance matrix $P(k)$ is defined as follows [71] :

$$P(k) = [\Phi(k)\Phi^T(k)]^{-1} = \left[\sum_{n=1}^{k} \varphi(n)\,\varphi^T(n)\right]^{-1} \tag{A.1}$$

The parameter estimate at the particular moment (k) can be rewritten as:

$$\hat{\theta}(k) = P(k)\left(\sum_{n=1}^{k} \varphi(n)\,y(n)\right) = P(k)\left[\left(\sum_{n=1}^{k-1} \varphi(n)\,y(n)\right) + \varphi(k)y(k)\right] \tag{A.2}$$

Similarly, the parameter estimate at the time instant (k-*1*) is defined as:

$$\hat{\theta}(k-1) = P(k-1)\left[\sum_{n=1}^{k-1} \varphi(n)\,y(n)\right] \tag{A.3}$$

Rearrange (A.3), the following is obtained:

$$\sum_{n=1}^{k-1} \varphi(n)\,y(n) = \; P^{-1}(k-1)\hat{\theta}(k-1) \tag{A.4}$$

According to the definition of the covariance matrix in (A.1) and using the form presented in (A.4), one can deduce the relationship between the inverse of the covariance matrix at (k-*1*) and its counterpart at (k) and substitute in (A.4) as follows:

$$P^{-1}(k-1) = \; P^{-1}(k) - \; \varphi(k)\varphi^T(k) \tag{A.5}$$

$$\sum_{n=1}^{k-1} \varphi(n)\,y(n) = \; [P^{-1}(k) - \; \varphi(k)\varphi^T(k)]\hat{\theta}(k-1) \tag{A.6}$$

From (A.2) and (A.6) the estimate at time k can now be written as:

$$\hat{\theta}(k) = \; P(k)\{[P^{-1}(k) - \; \varphi(k)\varphi^T(k)]\hat{\theta}(k-1) + \varphi(k)y(k)\} \tag{A.7}$$

$$\hat{\theta}(k) = \hat{\theta}(k-1) + \; P(k)\varphi(k)\left[y(k) - \; \varphi^T(k)\hat{\theta}(k-1)\right] \tag{A.8}$$

As illustrated in equation (A.8), the recursive estimation of the parameter vector $\hat{\theta}$ entails the computation of the covariance matrix $P(k)$ based on the matrix inversion given in (A.1) at each time instant. Therefore, a direct update from $P(k-1)$ to $P(k)$ in a recursive manner is required, and this can be achieved by means of a mathematical expression called the matrix inversion lemma [6]:

Matrix inversion lemma

$$(A+BCD)^{-1} = A^{-1} - A^{-1}B(C^{-1} + DA^{-1}B)^{-1}DA^{-1} \tag{A.9}$$

Assuming the matrices, *A*, *B*, *C*, and *D* with appropriate dimensions, and selecting $A = P^{-1}(k-1), B = \varphi(k), C = I,$ and $D = \varphi^T(k)$, hence using (A.5) the updated step for the covariance matrix can be written as:

$$P(k) = P(k-1) - \frac{P(k-1)\varphi(k)\varphi^T(k)P(k-1)}{I + \varphi^T(k)P(k-1)\varphi(k)} \tag{A.10}$$

The adaptation gain (Kalman gain) is the $N \times 1$ vector and is calculated as:

$$K(k) = P(k)\varphi(k) = \frac{P(k-1)\varphi(k)}{I + \varphi^T(k)P(k-1)\varphi(k)} \tag{A.11}$$

Using (A.8) and (A.11), the parameter estimate is computed as follows:

$$\hat{\theta}(k) = \hat{\theta}(k-1) + K(k)\left[y(k) - \varphi^T(k)\hat{\theta}(k-1)\right] \tag{A.12}$$

Appendix B. Simulink Model of the Proposed Structures

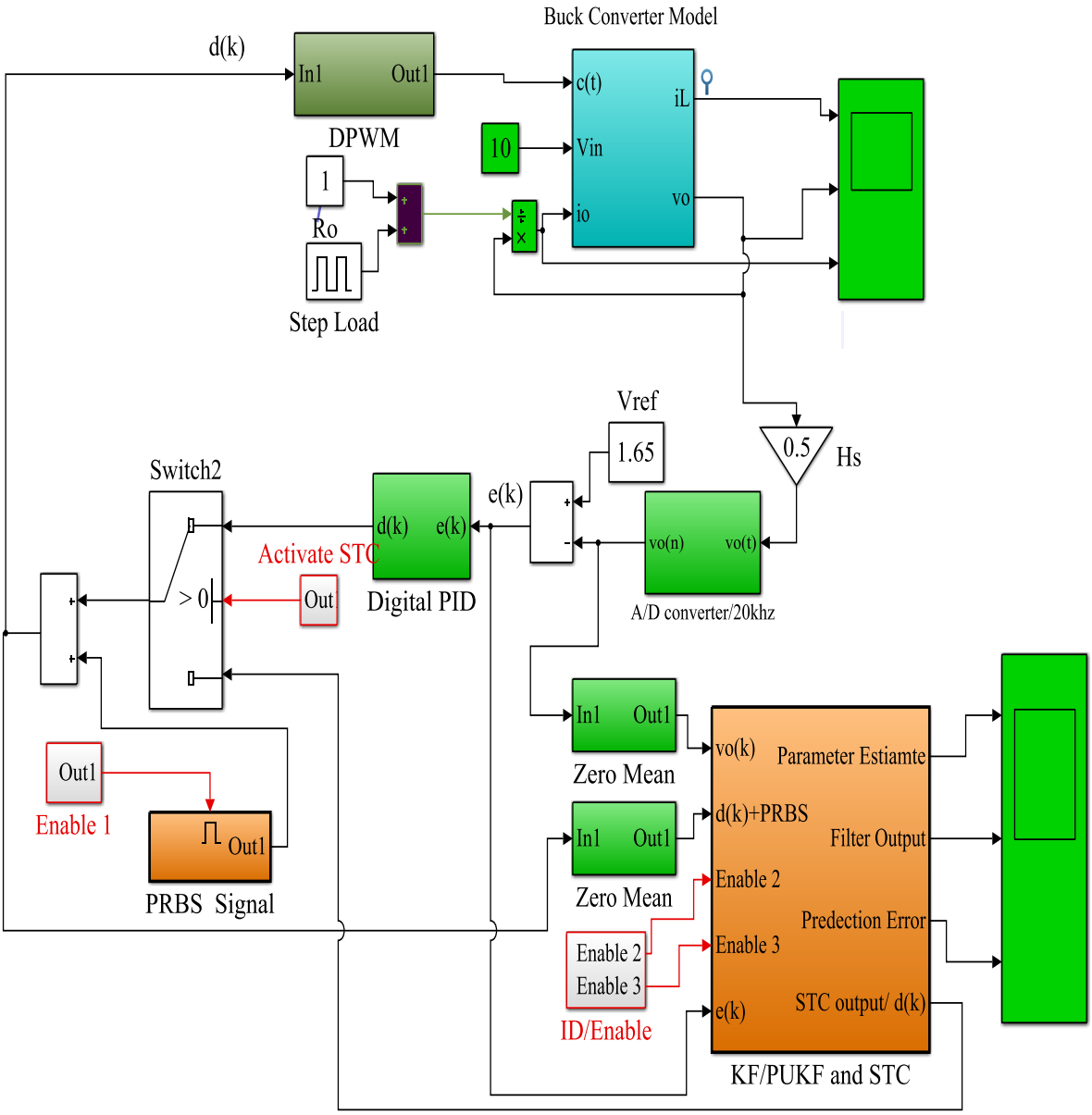

Figure B.1 Simulink model of parametric system identification using KF and STC based using PUKF

Appendix C. Developed Simulink Model for Real-Time Implementation

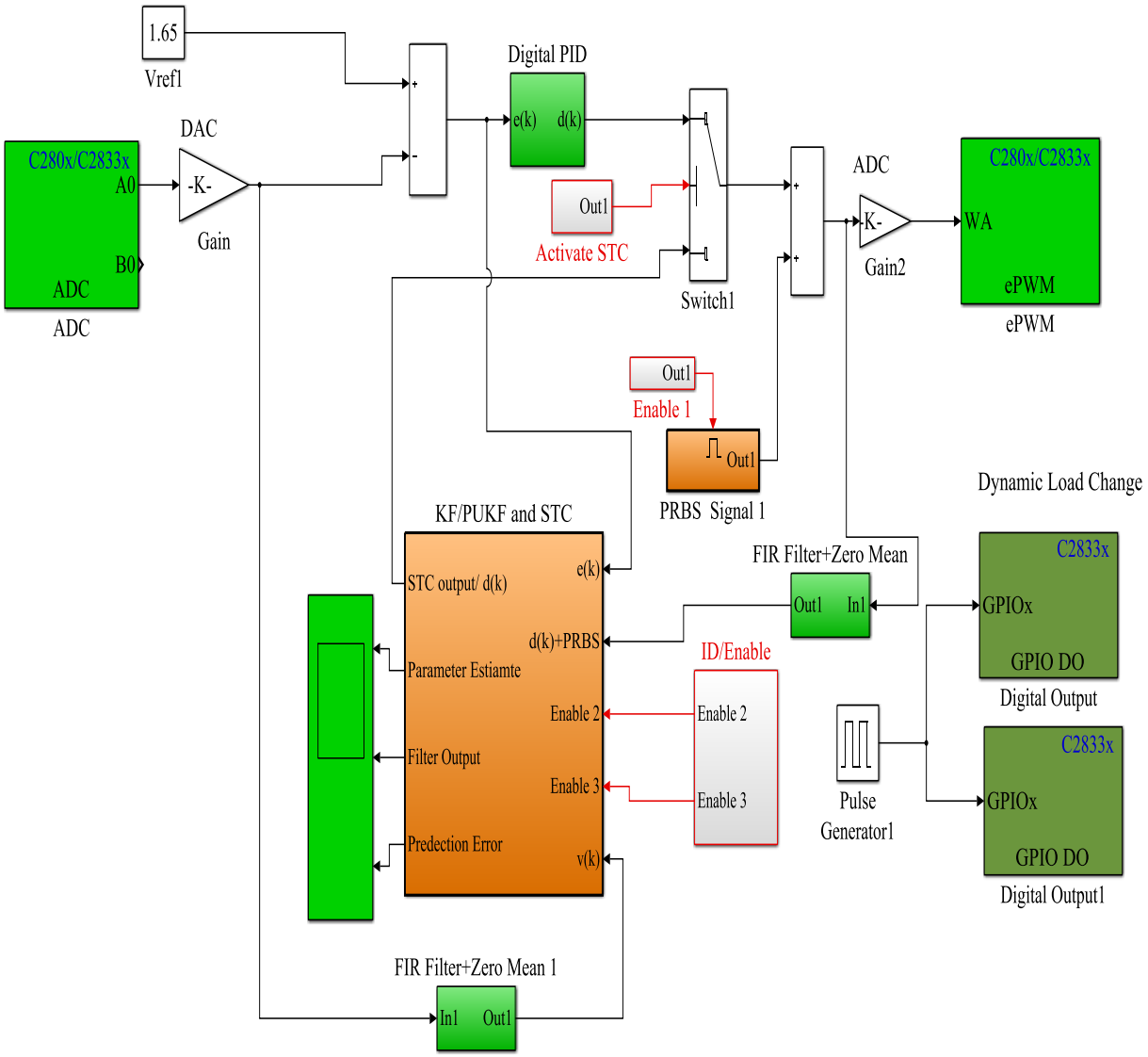

Figure C.1 Simulink model using Embedded Coder Support Package for Texas Instruments C2000 Processors

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